inputting of the corresponding write command regardless of whether tDSS is the shortest or the longest. The one-clock delay **619** is provided in order to insure that the write-amplifier-activation signal WRT and the column-selection pulse csp are not generated prior to a timing of the falling edge of the internal clock signal iCLK that corresponds to an end of the 1.5-cycle period.

In the first embodiment previously described, two address latches (latches **26** and **27**) are provided, whereas the second embodiment is provided with two sets of data latches. The number of these latches or the number of these data latches is not limited to two, but, as is apparent from the disclosure, may be more than two depending on the length of the longest tDSS.

In the following, third and fourth embodiments will be described.

In the first embodiment, two latches (i.e., the latches **26** and **27**) are provided for the purpose of latching addresses. Because of this, the case of the shortest tDDS as shown in FIG. **1** and the case of the longest tDDS as shown in FIG. **2** are properly dealt with. When the two bits (**D0**, **D1**) of the first data is supplied to the internal circuit, it is sufficient in the case of FIG. **1** to have a latch that stores a single address corresponding to the two-bit data. In the case of FIG. **2**, however, there is a need to have latches which store two addresses including a first address for the first two-bit data and a second address for second two-bit data. If only one latch is provided, the case of FIG. **2** cannot be handled. Namely, the address for the first two-bit data is rewritten by the address for the next data as the first two-bit data is transferred to the internal circuit, so that writing of data in specified memory cells cannot be achieved. Further, when the address latches are implemented via shift registers such as the address latches **61** and **62** of FIG. **12**, such a configuration cannot cope with the case of FIG. **1**. These shift registers perform a data-shift operation while holding a plurality of consecutive addresses (two addresses in this example). Because of this, an address cannot be output to the internal circuit for at least one clock cycle after the acquisition of the address. Namely, when the first two-bit data is transferred to the internal circuit, a corresponding address cannot be output from the shift register to the internal circuit.

The second embodiment is provided with two parallel sets of data latches (**51**, **52**, **53**; **54**, **55**, **56**) (see FIG. **12**). This configuration is necessary in order to cope with a case (FIG. **13**) in which two sets of data must remain intact in the storage when the first two-bit data is transferred to the internal circuit and a case (FIG. **14**) in which only one set of data needs to be kept in the storage.

In the examples of FIGS. **1** and **2** (or FIGS. **13** and **14**), a description was given with respect to a case in which the margin of the time period tDSS is equivalent to one clock cycle.

FIG. **23** is a timing chart for explaining timing relations between the clock signal, the data-strobe signal, and the data-write timings when the time period tDSS has a narrower margin (e.g, equivalent to half the clock cycle).

As is shown in the example of FIG. **23**, the address buffers must keep two addresses stored therein including an address for first two-bit data and an address for next two-bit data when the first two-bit data (**D0**, **D1**) is transferred to the internal circuit in parallel. In the example of FIG. **23**, there is only one pattern of timing relations as to how the addresses are acquired. Because of this, a configuration based on the address latch **61** plus the shift register **62** as described in connection with FIG. **12** can be employed as an address-buffer configuration in place of the configuration using the latch **26** plus the latch **27** as shown in FIG. **3**. It should be noted, however, that the shift register **62** of FIG. **12** delays an address signal by 1.5 clock cycles whereas the shift register in the third embodiment delays an address signal only by one clock cycle.

FIG. **24** is a block diagram of the third embodiment of the present invention. In FIG. **24**, the same elements as those of FIG. **3** are referred to by the sane numerals, and a description thereof will be omitted.

A semiconductor device **630** of FIG. **24** includes the data-input buffer **11**, the data latch **14**, the shift register **15**, the data latch **16**, the write amplifiers **29**, **30**, the odd-numbered-cell array **36**, the even-numbered-cell array **37**, the sense amplifiers **38**, **39**, the column decoders **40**, **41**, the read amplifiers **43**, **44**, the parallel-to-serial conversion unit **503**, the output buffer **504**, the data-strobe-input buffer **12**, the command decoder **22**, the write-command latch **23**, the mode register **502**, the burst-length-measurement counter **42**, the clock generator **501**, the write-pulse/column-selection-pulse generator **31**, the address buffer **13**, and the predecoders **34** and **35**.

The semiconductor device of FIG. **24** does not includes the increment latch **24**, the address generator **25**, the latches **26**, **27**, the address buffer **28**, the address generator **33**, the internal-clock generator **21**, the frequency dividers **17**, **18**, the latch-input-clock generator **20**, and the latch-output-clock generator **19**, all of which are shown in FIG. **3**. Instead, the semiconductor device of FIG. **24** includes an internal-clock generator **632** and an address generator **631**.

The internal-clock generator **632** has the same configuration as the internal-clock generator **60** of FIG. **12**, and the address generator **631** has a configuration that combines the address latch **61**, the shift register **62**, the address generator **25**, and the address buffer **28** of FIG. **12**.

With regard to the write-pulse/column-selection-pulse generator of FIG. **24**, the AND circuit **514** of FIG. **10** has one input thereof directly connected to the write-enable signal wrtz. Instead of this configuration, this input of the AND circuit **514** may be connected to the write-enable signal wrtz via such a one-clock delay as the one-clock delay **619** of FIG. **22**. In the third embodiment, the first two-bit data D0 and D1 are not supplied to the internal circuit until at least one clock cycle after the inputting of the corresponding write command regardless of the time period tDSS. It is desirable, therefore, to provide a one-clock-delay circuit in order to insure that a write pulse/column-selection pulse is not generated by accident due to noise in the data-strobe signal DS or the like within one clock cycle from the inputting of the write command.

In this manner, the third embodiment has a simpler structure than the first embodiment.

FIG. **25** is a block diagram of the fourth embodiment of the present invention.

The second embodiment of FIG. **12** is provided with the two sets of data latches so as to satisfy such timing conditions as required in the case of FIG. **13** and the case of FIG. **14**. When the tolerable margin of the time period tDSS is narrower than that of the second embodiment, there is a case in which it is sufficient for the data latches to hold only the first two-bit data at a moment when a corresponding address is output to the internal circuit 1.5 clock cycles after the acquisition of this address as shown in FIG. **14** regardless of where the actual time period tDSS is located within the tolerable margin. In such a case, one set of data latches (**14**, **15**, **16**) as in FIG. **3** may be used in place of the two sets of data latches (**51**, **52**, **53**; **54**, **55**, **56**) as shown in FIG. **12**.

In FIG. **25**, the same elements as those of FIG. **12** are referred to by the same numerals, and a description thereof will be omitted.

A semiconductor device **640** of FIG. **25** includes the data-input buffer **11**, the write amplifiers **29**, **30**, the odd-numbered-cell array **36**, the even-numbered-cell array **37**, the sense amplifiers **38**, **39**, the column decoders **40**, **41**, the read amplifiers **43**, **44**, the parallel-to-serial conversion unit **503**, the output buffer **504**, the data-strobe-input buffer **12**, the command decoder **22**, the write-command latch **23**, the mode register **502**, the burst-length-measurement counter **42**, the clock generator **501**, the write-pulse/column-selection-pulse generator **31**, the address buffer **13**, the predecoders **34**, **35**, and the internal-clock generator **60**.

The semiconductor device **640** of FIG. **25** does not include the data latch **51**, the shift register **52**, the data latch **53**, the data latch **54**, the shift register **55**, the data latch **56**, the delay circuit **57**, the frequency dividers **17**, **18**, the latch-input-clock generator **58**, and the latch-output-clock generator **59**, all of which are shown in FIG. **12**. Instead, the semiconductor device **640** includes a serial-to-parallel conversion unit **641** comprised of a data latch **642**, a shift register **643**, and a data latch **644**. The serial-to-parallel conversion unit **641** has the same configuration as the serial-to-parallel conversion unit **505** of the first embodiment shown in FIG. **3**

In this manner, the semiconductor memory device of the fourth embodiment has a simpler structure than does the second embodiment. In the fourth embodiment, just as in the second embodiment, addresses are acquired in synchronism with the clock signal, and data are acquired in synchronism with the data-strobe signal different from the clock signal, yet the internal circuit of the semiconductor device processes both the address and the data in synchronism with the clock signal.

Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese priority application No.10-022257 filed on Feb. 3, 1998, with Japanese Patent Office, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal, said semiconductor device comprising:

address-latch circuits which latches the addresses;

a first control circuit which selects one of said address-latch circuits in sequence in response to the clock signal, and controls the selected one of said address-latch circuits to latch a corresponding one of the addresses in response to the clock signal; and

a second control circuit which selects one of said address-latch circuits in sequence in response to the strobe signal, and controls the selected one of said address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

2. The semiconductor device as claimed in claim **1**, wherein said first control circuit includes a first frequency divider configured to divide a frequency of the clock signal, and selects one of said address-latch circuits in sequence by using the frequency-divided clock signal from said first frequency divider, and said second control circuit includes a second frequency divider configured to divide a frequency of the strobe signal, and selects one of said address-latch circuits in sequence by using the frequency-divided clock signal from said second frequency divider.

3. The semiconductor device as claimed in claim **1**, further comprising:

an increment-latch circuit which latches one of the addresses in synchronism with the clock signal; and

an address-generation circuit which increments the one of the addresses latched by said increment-latch circuit by 1, and supplies the incremented address to said address-latch circuits,

wherein each of said address-latch circuits configured so as to be capable of selecting the corresponding one of the addresses externally provided or the incremented address supplied from said address-generation circuit for the latching operation thereof.

4. The semiconductor device as claimed in claim **1**, further comprising an address buffer, wherein said address-latch circuits supply the addresses to said address buffer without a clock-cycle delay during a read operation.

5. The semiconductor device as claimed in claim **1**, further comprising data-latch circuits, each of which latches a corresponding datum of the data in synchronism with the strobe signal, and outputs the corresponding datum of the data in synchronism with the strobe signal.

6. The semiconductor device as claimed in claim **5**, wherein said data-latch circuits operate in response to a write-enable signal which is generated in response to a write command to said semiconductor device.

7. The semiconductor device as claimed in claim **6**, wherein the write-enable signal controls said first control circuit and said second control circuit to operate for a predetermined time period after receiving the write command.

8. The semiconductor device as claimed in claim **5**, wherein said data-latch circuit comprises:

a first data-latch circuit which latches a corresponding datum of the data in synchronism with a rising edge of the strobe signal; and

a second data-latch circuit which latches a corresponding datum of the data in synchronism with a falling edge of the strobe signal.

9. A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal, said semiconductor device comprising:

data-latch circuits;

a first control circuit which selects one of said data-latch circuits in sequence in response to the strobe signal, and controls the selected one of said data-latch circuits to latch a corresponding datum of the data in response to the strobe signal; and

a second control circuit which selects one of said data-latch circuits in sequence in response to the clock signal, and controls the selected one of said data-latch circuits to output a corresponding datum of the data in response to the clock signal.

10. The semiconductor device as claimed in claim **9**, wherein said first control circuit includes a first frequency divider configured to divide a frequency of the strobe signal, and selects one of said data-latch circuits in sequence by using the frequency-divided strobe signal from said first frequency divider, and said second control circuit includes a second frequency divider configured to divide a frequency of the clock signal, and selects one of said data-latch circuits in sequence by using the frequency-divided clock signal from said second frequency divider.

11. The semiconductor device as claimed in claim 9, wherein each of said data-latch circuits includes:

a first latch which latches a corresponding datum of the data in synchronism with a rising edge of the strobe signal; and

a second latch which latches a corresponding datum of the data in synchronism with a falling edge of the strobe signal.

12. The semiconductor device as claimed in claim 9, wherein said address-latch circuit operates in response to a write-enable signal which is generated in response to a write command to said semiconductor device.

13. The semiconductor device as claimed in claim 12, wherein the write-enable signal controls said first control circuit and said second control circuit to operate for a predetermined time period after receiving the write command.

14. The semiconductor device as claimed in claim 9, further comprising an address-latch circuit which latches the addresses in sequence in synchronism with the clock signal, and outputs the addresses in synchronism with the clock signal.

15. The semiconductor device as claimed in claim 14, further comprising

an address-generation circuit which increments one of the addresses latched by said address-latch circuit, and supplies the incremented address to said address-latch circuit,

wherein said address-latch circuit is configured so as to be capable of selecting the addresses externally provided or the incremented address supplied from said address-generation circuit for the latching operation thereof.

16. The semiconductor device as claimed in claim 14, wherein said address-latch circuit includes a delay circuit which delays output timings of the addresses by a predetermined number of cycles of the clock signal.

17. The semiconductor device as claimed in claim 14, further comprising an address buffer, wherein said address-latch circuit supplies the addresses to said address buffer without a clock-cycle delay during a read operation.

18. A memory circuit receiving a clock signal and a strobe signal which have an identical cycle but have independent timings, comprising:

an address-input circuit which latches address signals in response to the clock signal, and outputs the address signals in response to a timing signal;

a data-input circuit which latches data signals in response to the strobe signal, and outputs the data signals in response to said timing signal; and

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied form the address-input circuit.

19. The memory circuit as claimed in claim 18, wherein said data-input circuit latches the data signals in synchronism with rising edges and falling edges of the strobe signal.

20. The memory circuit as claimed in claim 18, wherein said timing signal is responsive to the strobe signal.

21. The memory circuit as claimed in claim 20, wherein the address-input circuit includes:

a first latch circuit which latches the address signal in response to a first rising edge of the clock signal, and outputs the address signal in response to the timing signal; and

a second latch circuit, connected in parallel to the first latch circuit, which latches next address signal in response to a next rising edge of the clock signal, and outputs the next address signal in response to the timing signal.

22. The memory circuit as claimed in claim 21, wherein the address-input circuit outputs the address signal prior to outputting the next address signal.

23. The memory circuit as claimed in claim 20, wherein said address-input circuit includes a shift register which operates in response to the clock signal.

24. A method of writing data in the memory circuit of claim 23, comprising a step of adjusting an input timing of the strobe signal relative to the clock signal such that said shift register stores two addresses at a time when the data-input circuit outputs the data signals.

25. The memory circuit as claimed in claim 20, further comprising:

a decode circuit which receives the address signal from the address-input circuit, and decodes the address signal in response to a first activation signal; and

a write amplifier which receives the data signal from the data-input circuit, and amplifies the data signal in response to a second activation signal in a data-write mode,

wherein both of the first and second activation signals are responsive to the strobe signal in the data-write mode.

26. The memory circuit as claimed in claim 25, wherein in a data-read mode, the first activation signal is responsive to the clock signal, and the second activation signal is in a deactivated state.

27. The memory circuit as claimed in claim 25, wherein in the data-write mode, the first activation signal activates said decode circuit after said address-input circuit outputs the address signals, and the second activation signal activates said write amplifier after said data-input circuit outputs the data signals.

28. The memory circuit as claimed in claim 18, wherein said timing signal is responsive to the clock signal.

29. The memory circuit as claimed in claim 28, wherein said data-input circuit includes:

a first data-input circuit which latches the data signals in sequence in response to a first rising edge and a first falling edge of the strobe signal, and outputs the data signals in parallel in response to the timing signal; and

a second data-input circuit, connected in parallel to the first data-input circuit, which latches next data signals in sequence in response to a next rising edge and a next falling edge of the strobe signal, and outputs the next data signals in parallel in response to the timing signal.

30. The memory circuit as claimed in claim 29, wherein said data-input circuit outputs the data signals prior to outputting the next data signals.

31. The memory circuit as claimed in claim 28, wherein said data-input circuit includes a first data-input circuit which latches the data signals in sequence in response to a rising edge and a falling edge of the strobe signal, and outputs the data signals in parallel in response to the timing signal.

32. The memory circuit as claimed in claim 31, wherein said first data-input circuit latches next data signals after outputting the data signals.

33. The memory circuit as claimed in claim 28, wherein said address-input circuit includes a shift register which operates in response to the clock signal.

34. The memory circuit as claimed in claim 33, wherein said shift register delays the address signals by 1.5 clock cycles of the clock signal.

35. The memory circuit as claimed in claim **28**, further comprising:

a decode circuit which receives the address signal from the address-input circuit, and decodes the address signal in response to a first activation signal; and

a write amplifier which receives the data signal from the data-input circuit, and amplifies the data signal in response to a second activation signal in a data-write mode,

wherein both of the first and second activation signals are responsive to the clock signal in the data-write mode.

36. The memory circuit as claimed in claim **39**, wherein in a data-read mode, the first activation signal is responsive to the clock signal, and the second activation signal is in a deactivated state.

37. The memory circuit as claimed in claim **35**, wherein in the data-write mode, the first activation signal activates said decode circuit after said address-input circuit outputs the address signals, and the second activation signal activates said write amplifier after said data-input circuit outputs the data signals.

38. The memory circuit as claimed in claim **18**, wherein a timing at which said address-input circuit outputs the address signals is concurrent with a timing at which said data-input circuit outputs the data signals corresponding to the address signals.

39. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and

the strobe signal has a cycle identical to that of the clock signal, and a first timing of a first rising edge of the strobe signal is different from a second timing of a corresponding rising edge of the clock signal.

40. The memory circuit as claimed in claim **39**, wherein the first timing is later than the second timing with a timing gap therebetween being shorter than one cycle of the clock signal.

41. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal, said address-input circuit includes a shift register which operates in response to the clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit;

said timing signal is responsive to the clock signal; and

a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.

42. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a timing signal, the address-input circuit includes a shift register which operates in response to the clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the timing signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit;

the said timing signal is responsive to the strobe signal; and

a bypass circuit provided in parallel to said shift register, wherein the address signals pass through the bypass circuit and bypass said shift register in a data-read mode.

* * * * *

EXHIBIT S

US006320819B2

(12) **United States Patent**
Tomita et al.

(10) **Patent No.: US 6,320,819 B2**
(45) **Date of Patent: Nov. 20, 2001**

(54) **SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS**

(75) Inventors: **Hiroyoshi Tomita; Tatsuya Kanda,** both of Kawasaki (JP)

(73) Assignee: **Fujitsu Limited,** Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/733,961**

(22) Filed: **Dec. 12, 2000**

Related U.S. Application Data

(62) Division of application No. 09/240,007, filed on Jan. 29, 1999.

(30) **Foreign Application Priority Data**

Feb. 3, 1998 (JP) 10-022257

(51) **Int. Cl.**[7] **G11C 8/00**
(52) **U.S. Cl.** **365/233**; 365/189.05; 365/230.08; 365/194
(58) **Field of Search** 365/233, 189.05, 365/230.08, 194

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Primary Examiner—Huan Hoang
(74) *Attorney, Agent, or Firm*—Arent Fox Kintner Plotkin & Kahn PLLC

(57) **ABSTRACT**

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

6 Claims, 25 Drawing Sheets

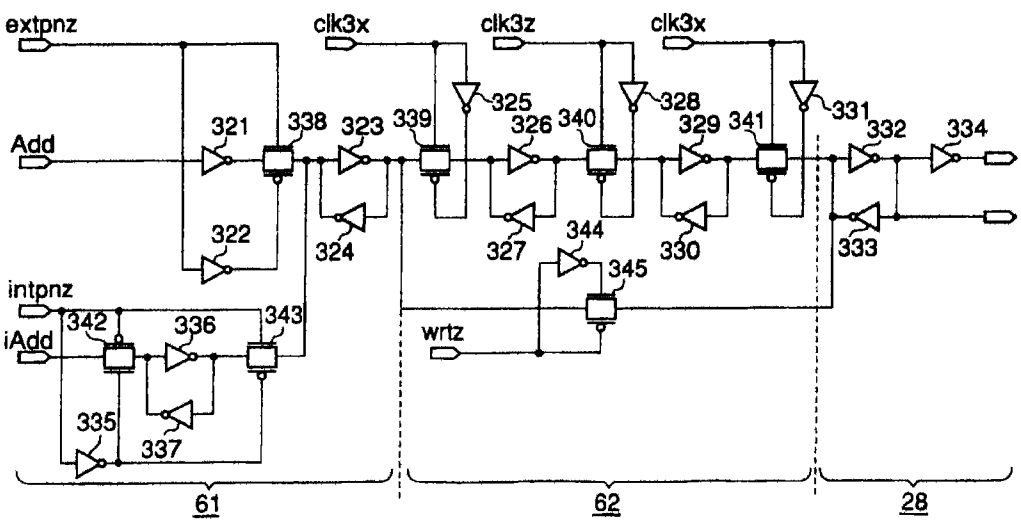


FIG. 1

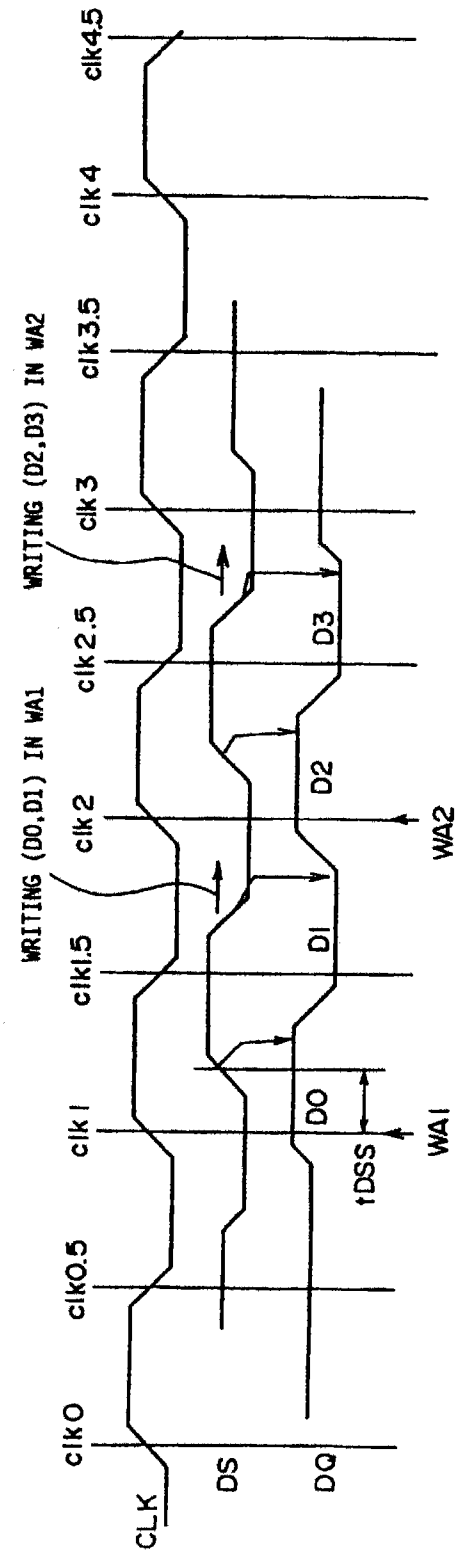

clk4.5
clk4
clk3.5
clk3
clk2.5
clk2
clk1.5
clk1
clk0.5
clk0
CLK
DS
DQ
WRITING (D2,D3) IN WA2
WRITING (D0,D1) IN WA1
D3
D2
D1
D0
WA2
WA1
tDSS

FIG. 2

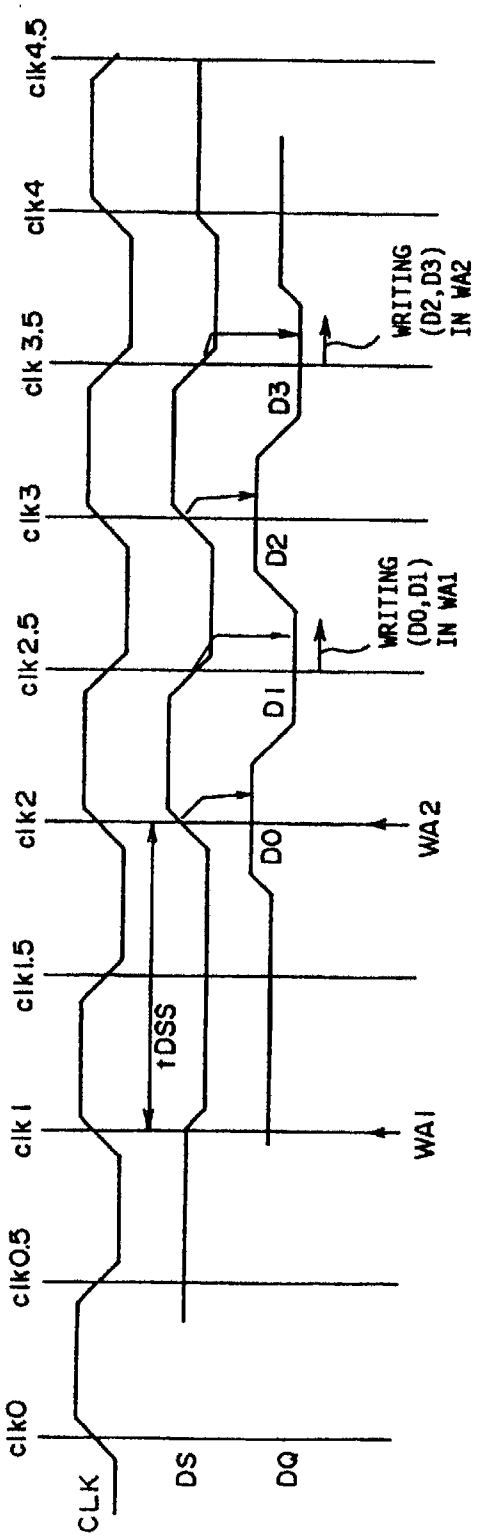
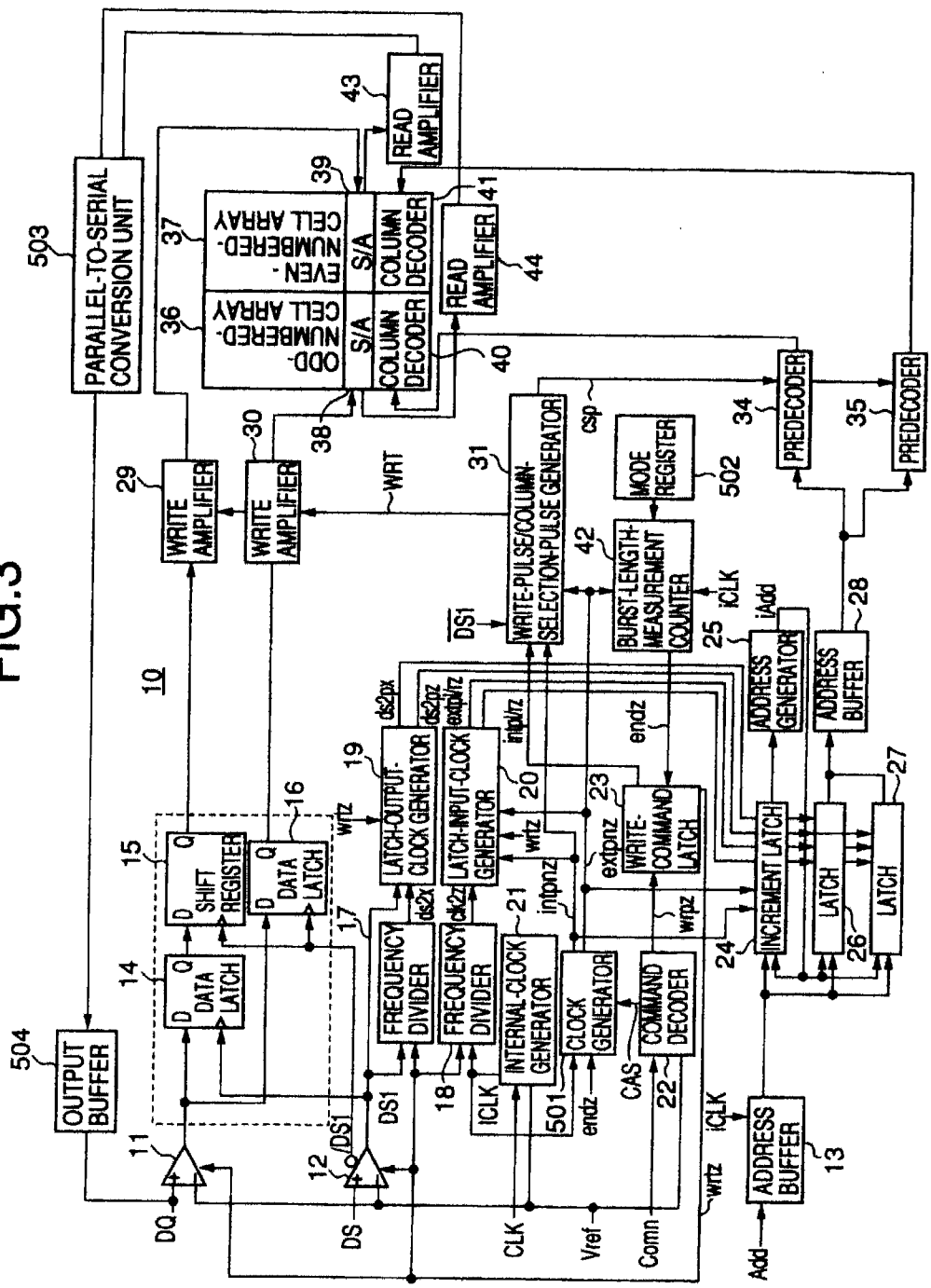

clk4.5
clk4
clk 3.5
clk3
clk2.5
clk2
clk1.5
clk1
clk0.5
clk0
CLK
DS
DQ
WRITING (D2,D3) IN WA2
WRITING (D0,D1) IN WA1
D3
D2
D1
D0
WA2
WA1
tDSS

FIG.3


PARALLEL-TO-SERIAL CONVERSION UNIT
503
READ AMPLIFIER
43
ODD-NUMBERED-CELL ARRAY
EVEN-NUMBERED-CELL ARRAY
S/A
COLUMN DECODER
39
41
37
36
40
44
READ AMPLIFIER
PREDECODER
34
35
WRITE AMPLIFIER
29
30
WRT
38
31
WRITE-PULSE/COLUMN-SELECTION-PULSE GENERATOR
csp
MODE REGISTER
502
42
BURST-LENGTH-MEASUREMENT COUNTER
25
iCLK
iAdd
ADDRESS GENERATOR
ADDRESS BUFFER
28
10
DS1
LATCH-OUTPUT-CLOCK GENERATOR
LATCH-INPUT-CLOCK GENERATOR
19
20
23
WRITE-COMMAND LATCH
INCREMENT LATCH
LATCH
LATCH
27
26
24
SHIFT REGISTER
DATA LATCH
DATA LATCH
15
16
14
17
FREQUENCY DIVIDER
FREQUENCY DIVIDER
INTERNAL-CLOCK GENERATOR
CLOCK GENERATOR
COMMAND DECODER
21
18
501
22
CAS
OUTPUT BUFFER
504
11
12
ADDRESS BUFFER
13
DQ
DS
CLK
Vref
Comn
Add

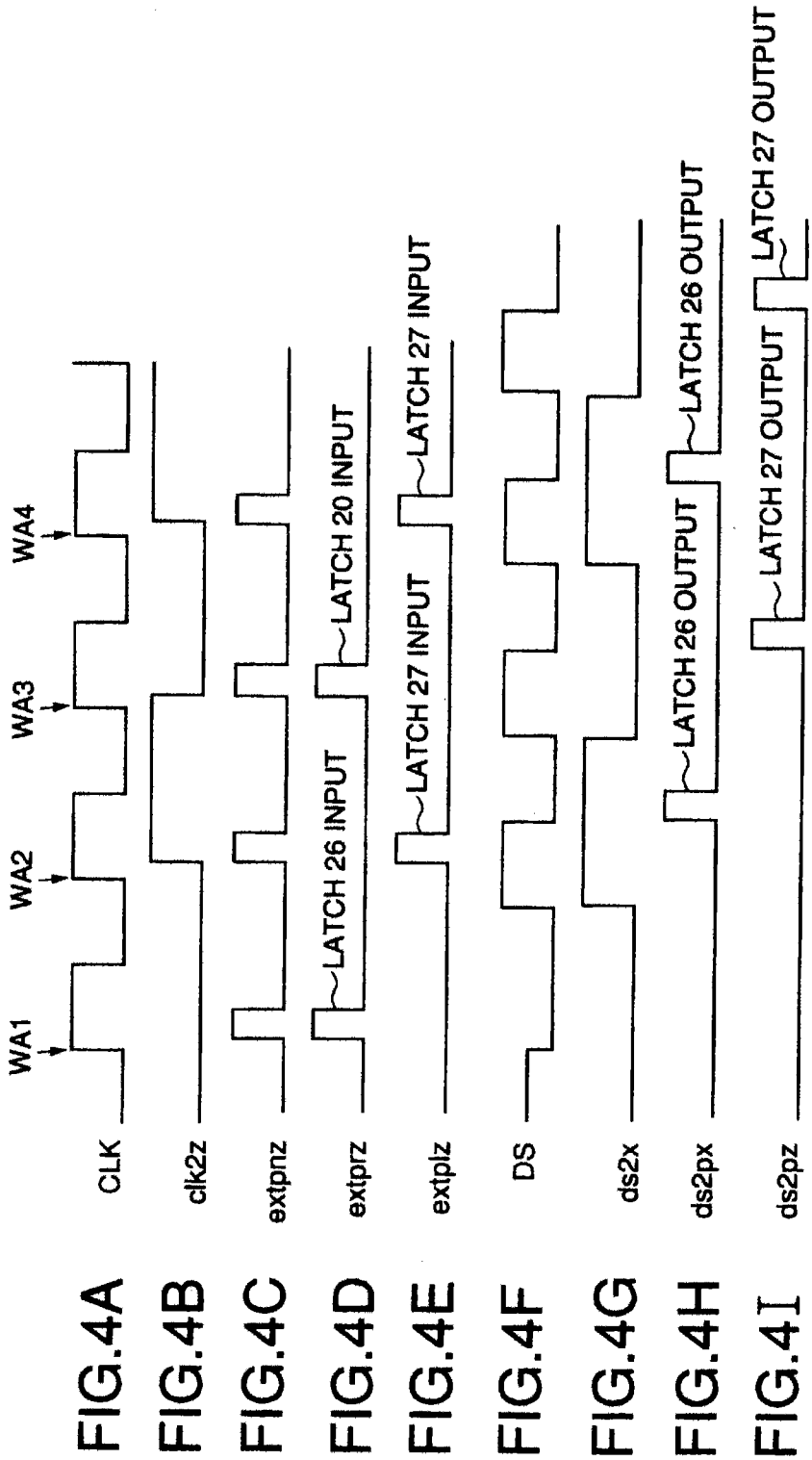


FIG.4A FIG.4B FIG.4C FIG.4D FIG.4E FIG.4F FIG.4G FIG.4H FIG.4I

FIG.5

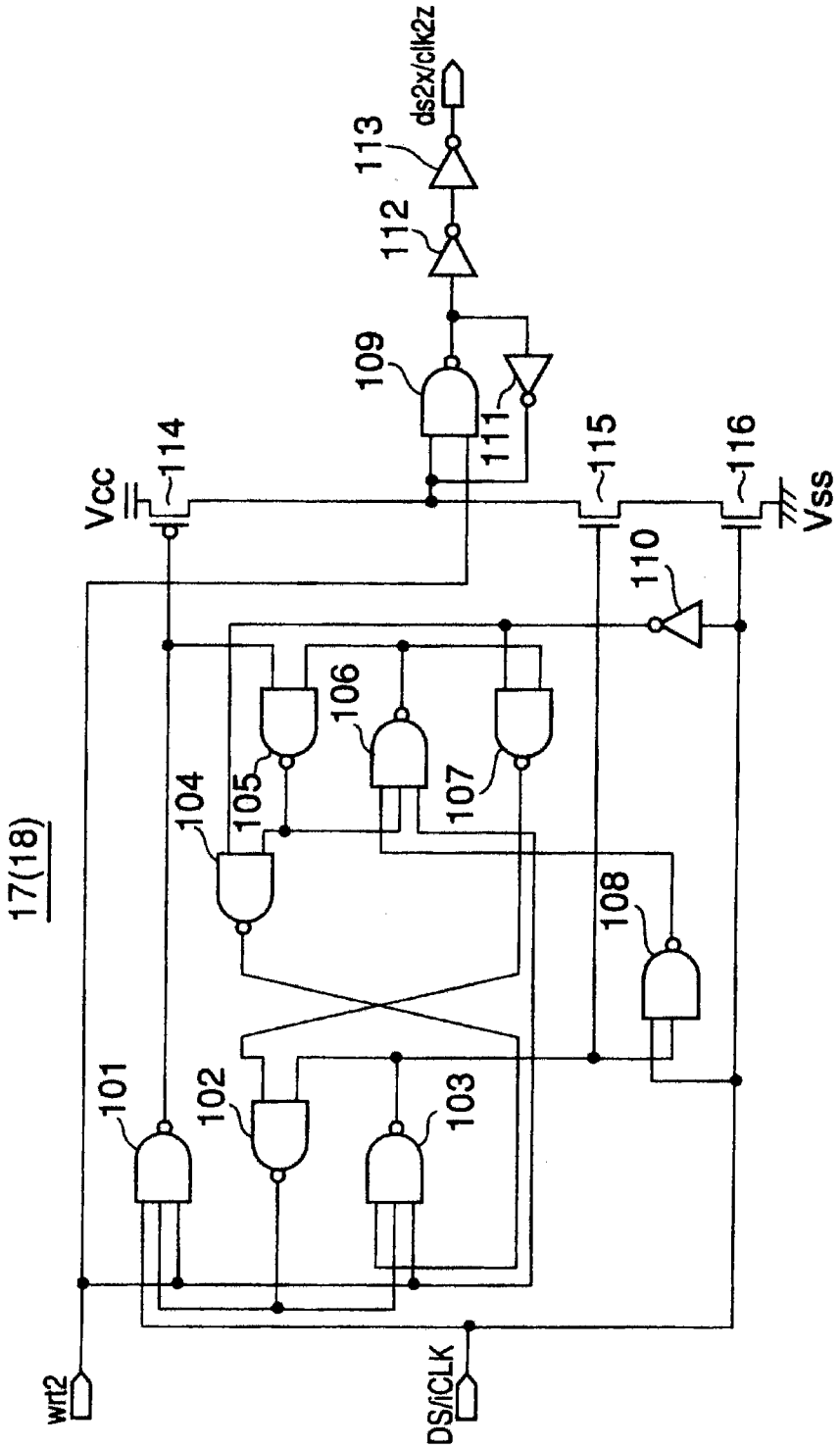

ds2x/clk2z
113
112
109
111
114
115
116
Vcc
Vss
110
106
104
105
107
17(18)
108
101
102
103
wrt2
DS/ICLK

FIG.6

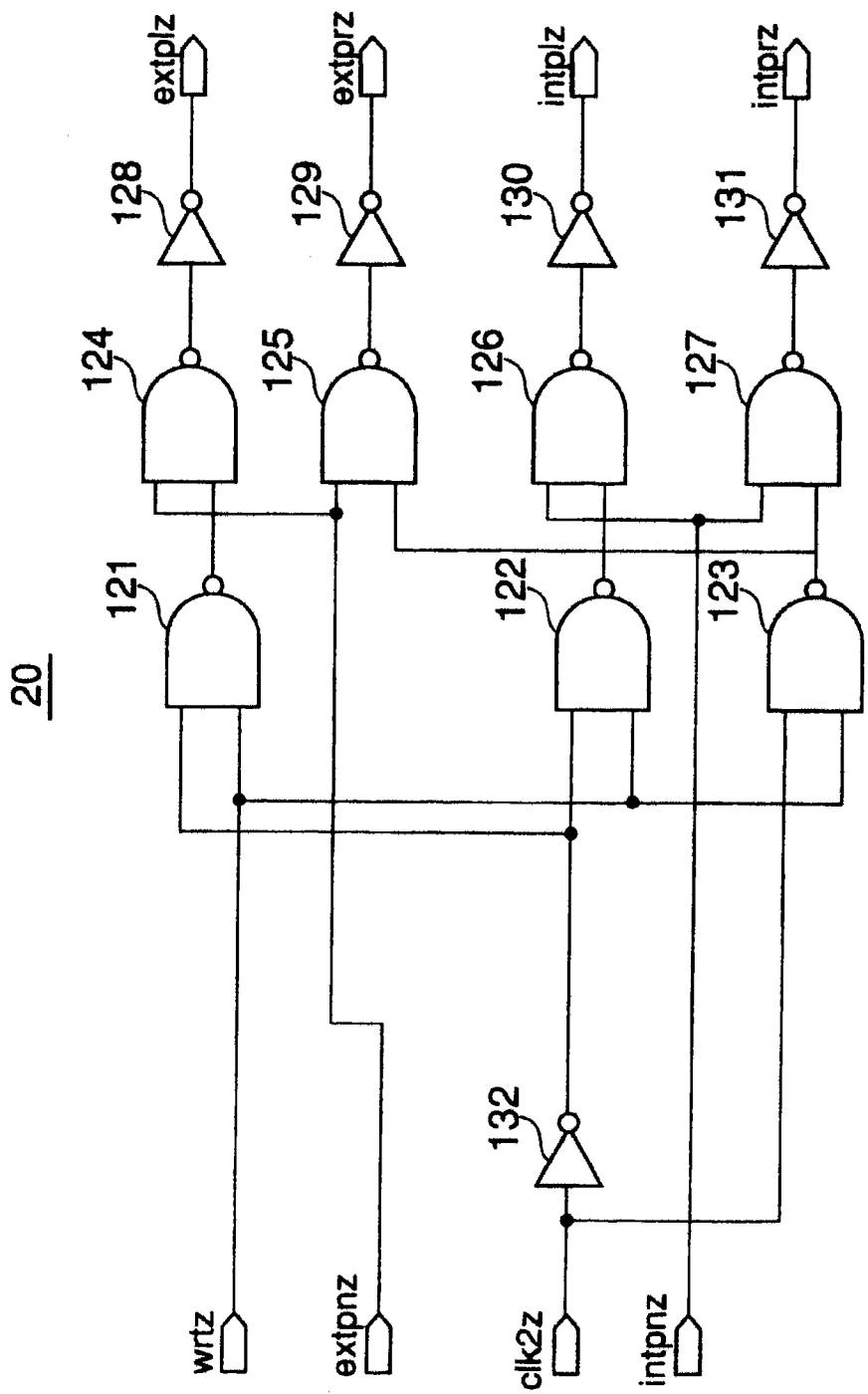

20
extplz
extprz
intplz
intprz
128
129
130
131
124
125
126
127
121
122
123
132
wrtz
extpnz
clk2z
intpnz

FIG.7

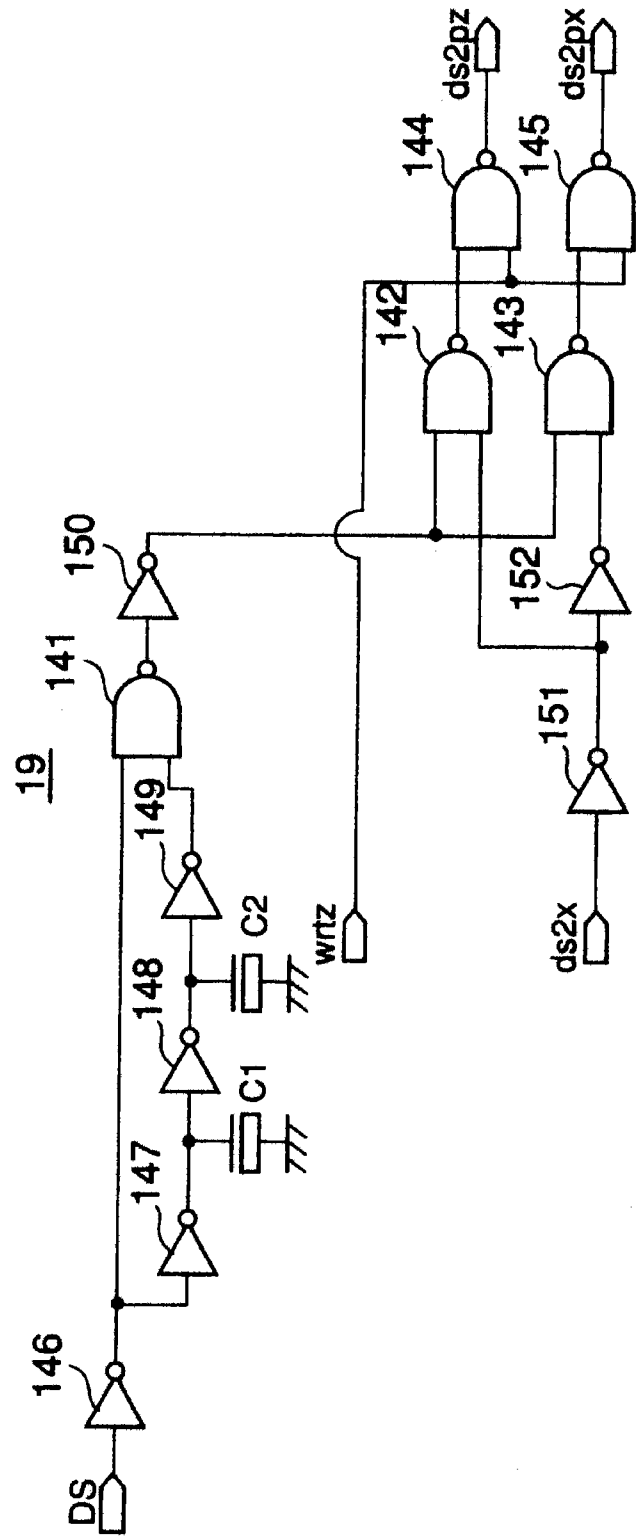

ds2pz
ds2px
144
145
142
143
150
152
141
19
151
149
C2
wrtz
ds2x
148
C1
147
146
DS

FIG.8

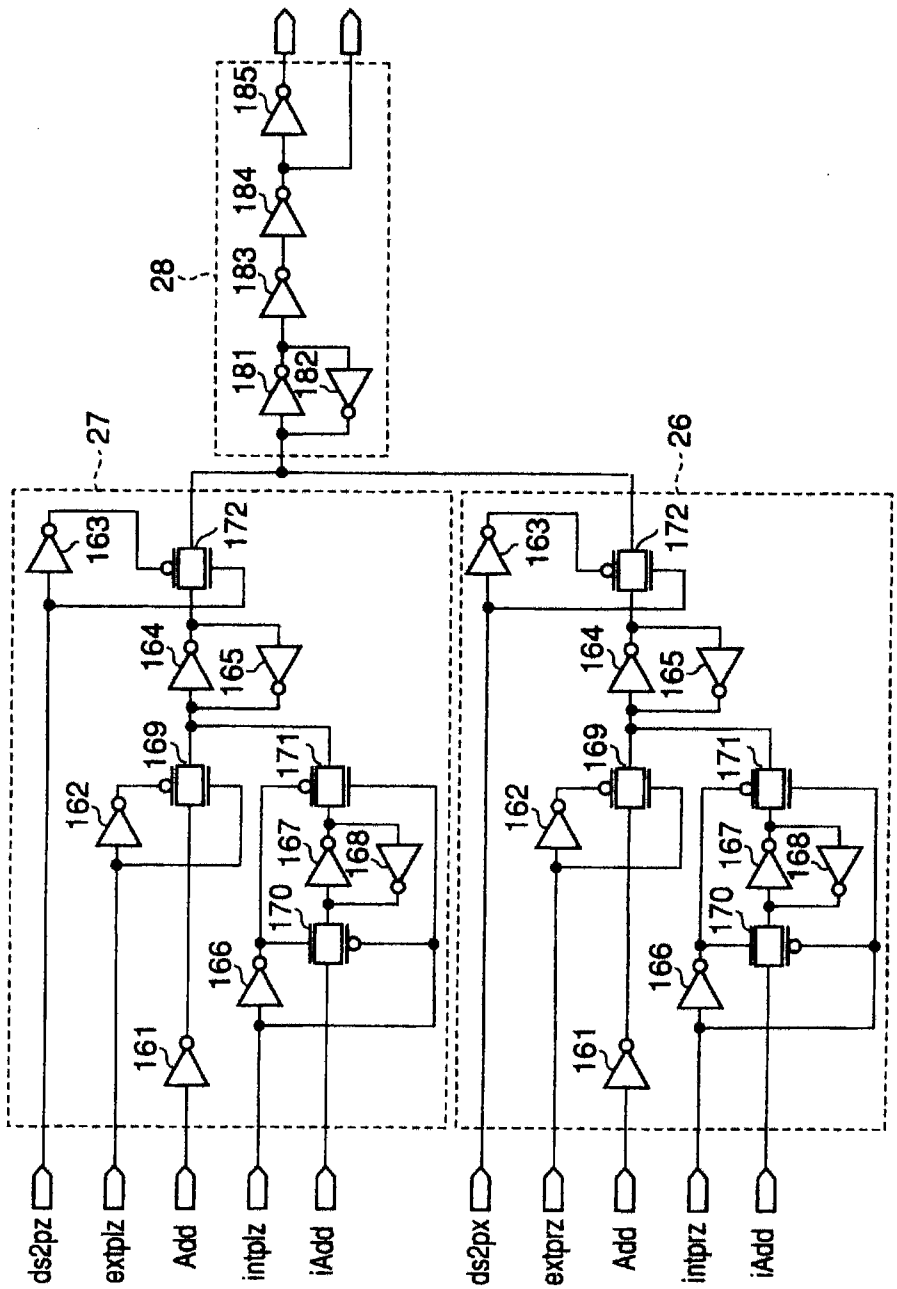

28
27
26
185
184
183
181
182
163
172
164
165
169
171
162
167
168
170
166
161
ds2pz
extplz
Add
intplz
iAdd
ds2px
extprz
Add
intprz
iAdd

FIG.9

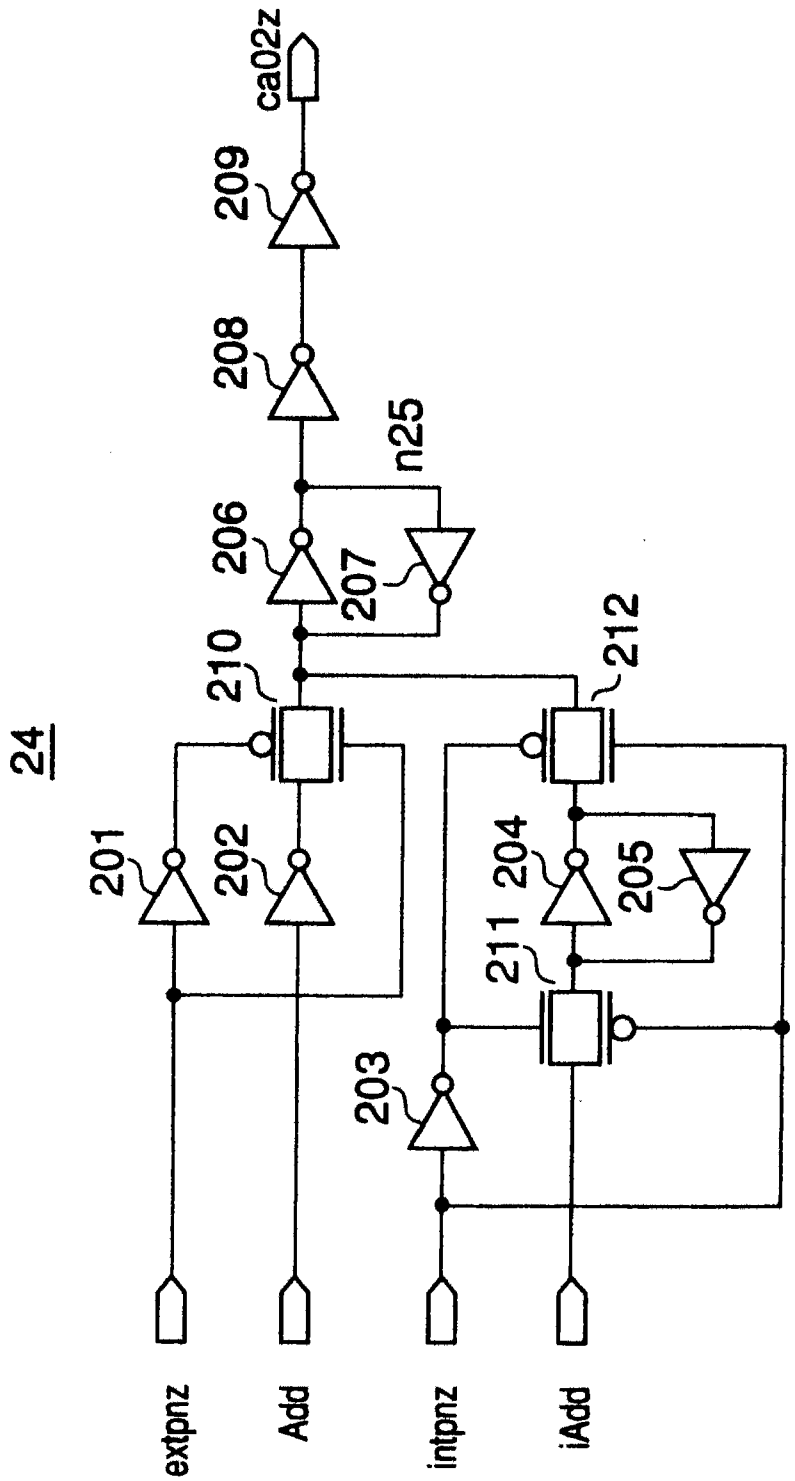
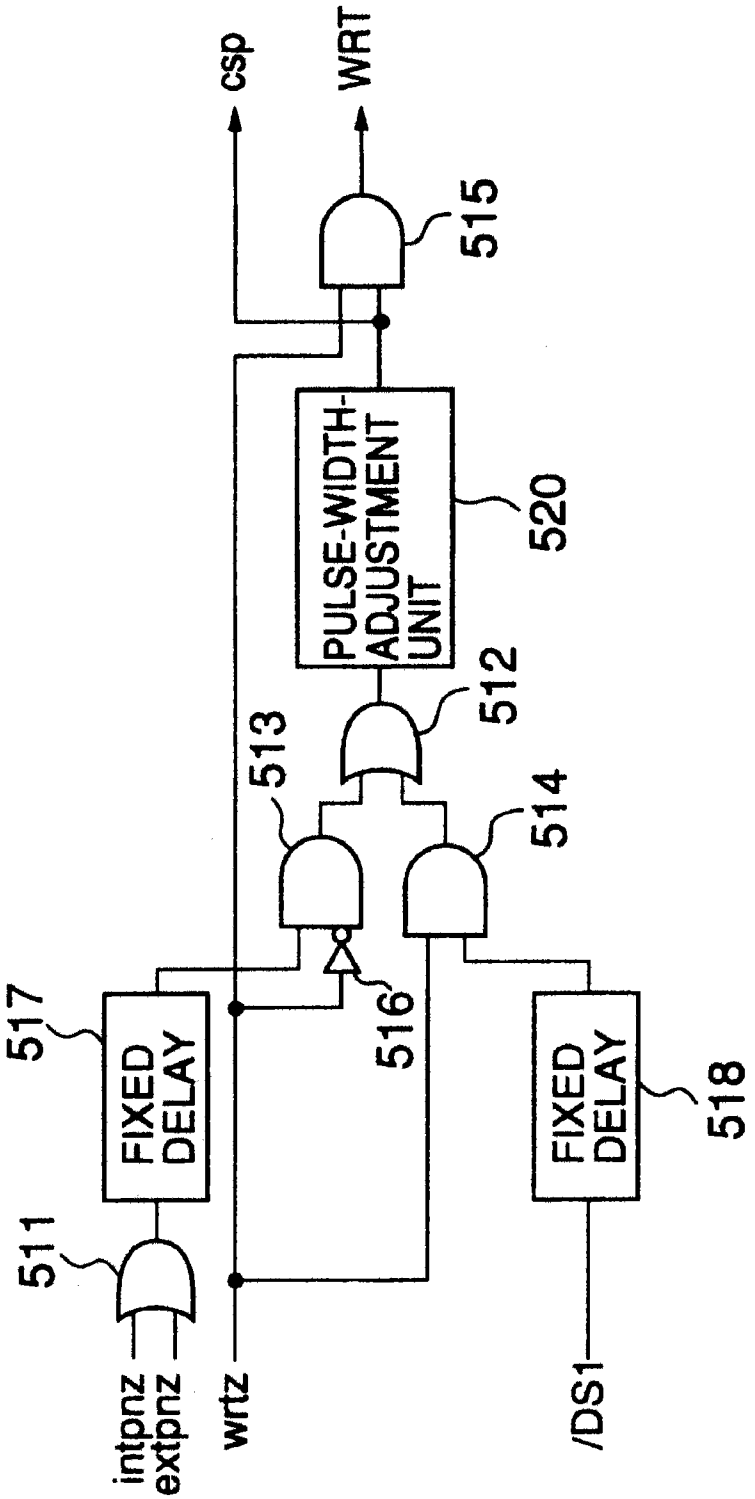

24
ca02z
209
208
n25
206
207
210
212
201
202
204
205
211
203
extpnz
Add
intpnz
iAdd

FIG.10


csp
WRT
515
PULSE-WIDTH-ADJUSTMENT UNIT
520
512
513
514
516
517
FIXED DELAY
FIXED DELAY
518
511
intpnz
extpnz
wrtz
/DS1

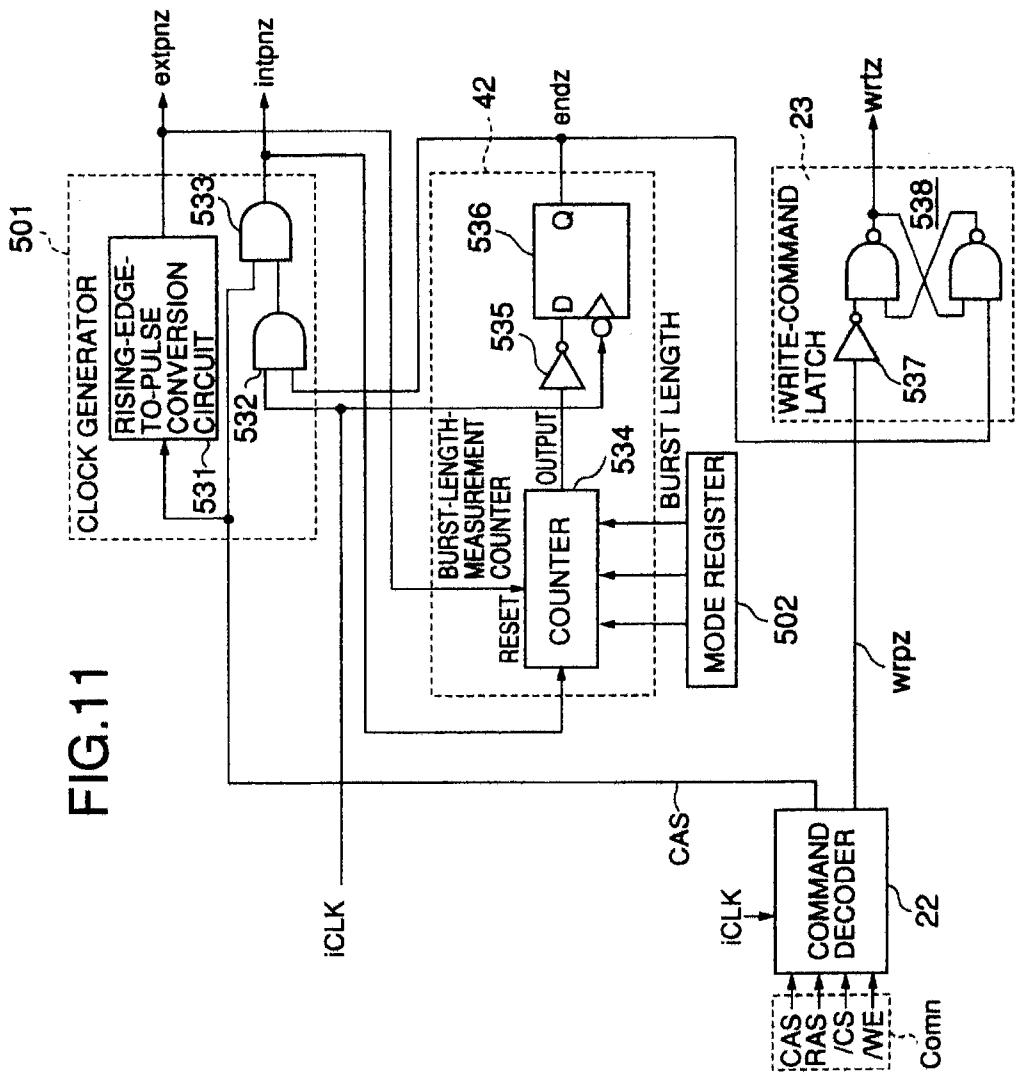

501
CLOCK GENERATOR
RISING-EDGE-TO-PULSE CONVERSION CIRCUIT
531
532
533
extpnz
intpnz
iCLK
42
endz
536
Q
D
535
BURST-LENGTH-MEASUREMENT COUNTER
OUTPUT
534
RESET
COUNTER
BURST LENGTH
MODE REGISTER
502
23
wrtz
WRITE-COMMAND LATCH
538
537
wrpz
CAS
iCLK
COMMAND DECODER
22
/CAS
/RAS
/CS
/WE
Comn

FIG.11

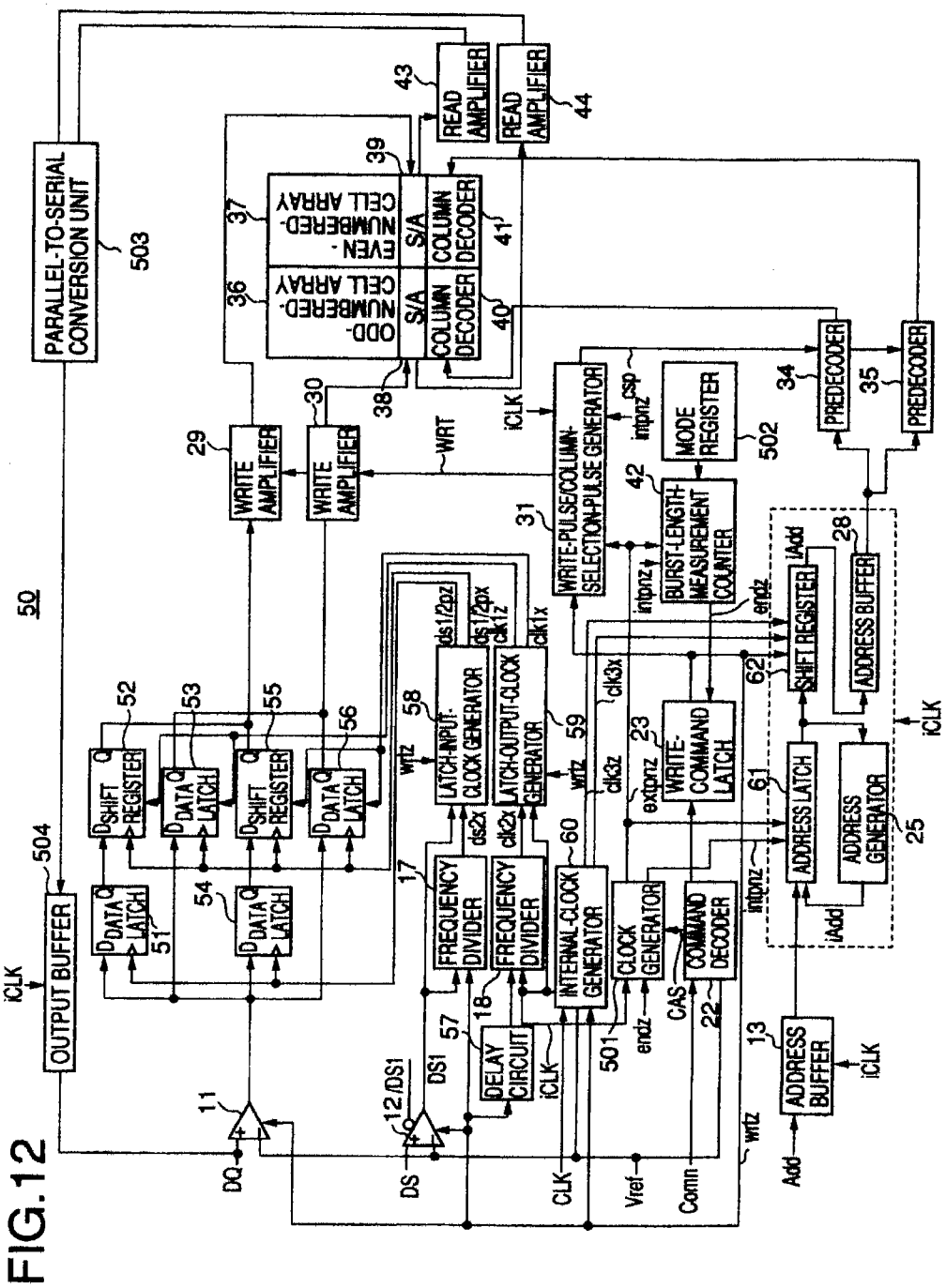

PARALLEL-TO-SERIAL CONVERSION UNIT
503
READ AMPLIFIER
READ AMPLIFIER
ODD-NUMBERED-CELL ARRAY
EVEN-NUMBERED-CELL ARRAY
S/A
COLUMN DECODER
WRITE AMPLIFIER
WRITE AMPLIFIER
WRT
iCLK
csp
intpnz
MODE REGISTER
502
PREDECODER
PREDECODER
WRITE-PULSE/COLUMN-SELECTION-PULSE GENERATOR
BURST-LENGTH-MEASUREMENT COUNTER
endz
SHIFT REGISTER
ADDRESS BUFFER
iAdd
50
DATA LATCH
SHIFT REGISTER
LATCH-INPUT-CLOCK GENERATOR
LATCH-OUTPUT-CLOCK GENERATOR
wrtz
WRITE-COMMAND LATCH
extpnz
ADDRESS LATCH
ADDRESS GENERATOR
504
OUTPUT BUFFER
FREQUENCY DIVIDER
INTERNAL-CLOCK GENERATOR
CLOCK GENERATOR
COMMAND DECODER
CAS
DELAY CIRCUIT
DS1
ADDRESS BUFFER
DQ
DS
CLK
Vref
Comn
Add
FIG.12

FIG. 13

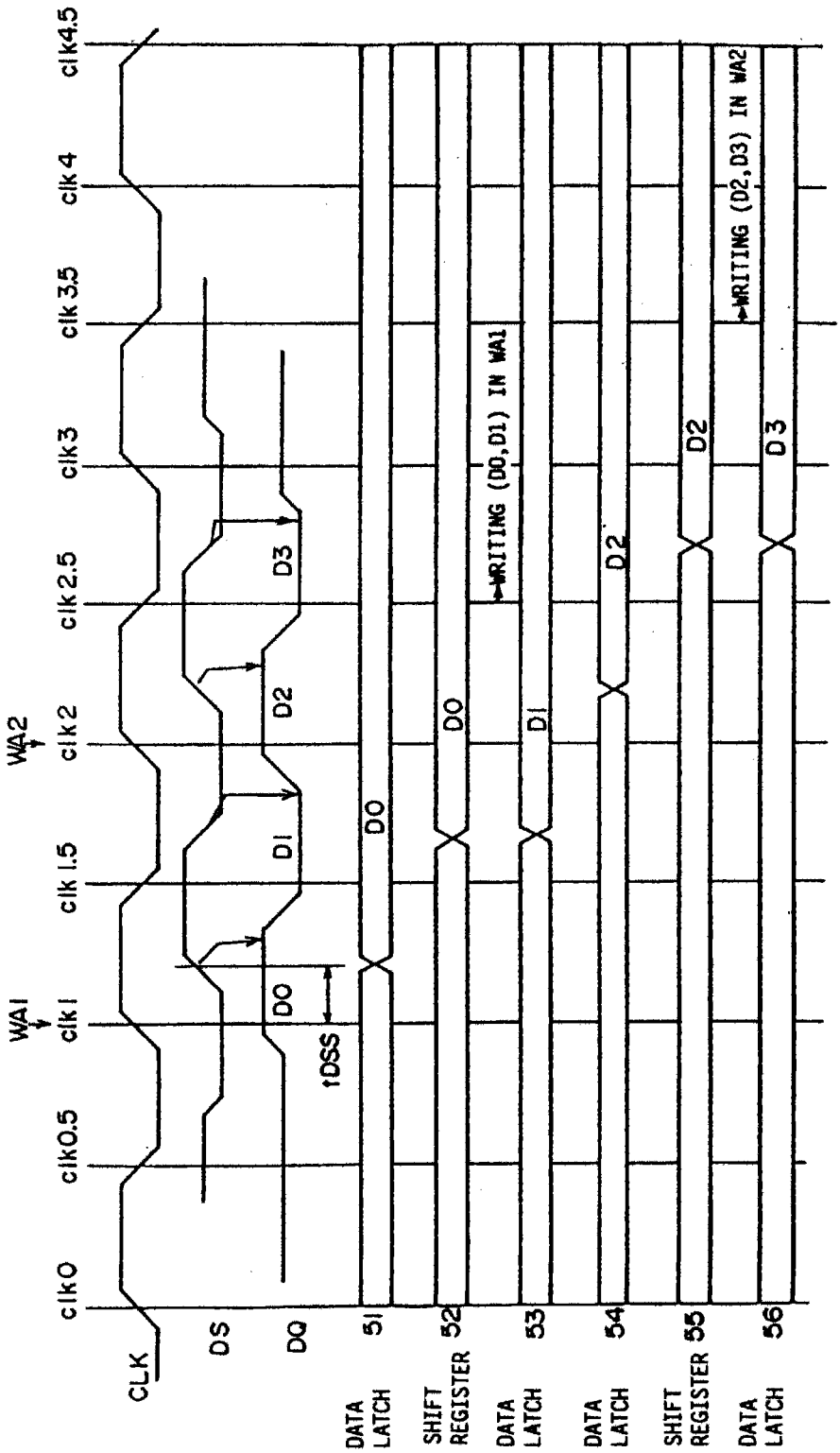

clk4.5
clk4
clk3.5
clk3
clk2.5
clk2
clk1.5
clk1
clk0.5
clk0
WA2
WA1
CLK
DS
DQ
D3
D2
D1
D0
tDSS
WRITING (D0,D1) IN WA1
WRITING (D2,D3) IN WA2
51
52
53
54
55
56
DATA LATCH
SHIFT REGISTER
DATA LATCH
DATA LATCH
SHIFT REGISTER
DATA LATCH

FIG. 14

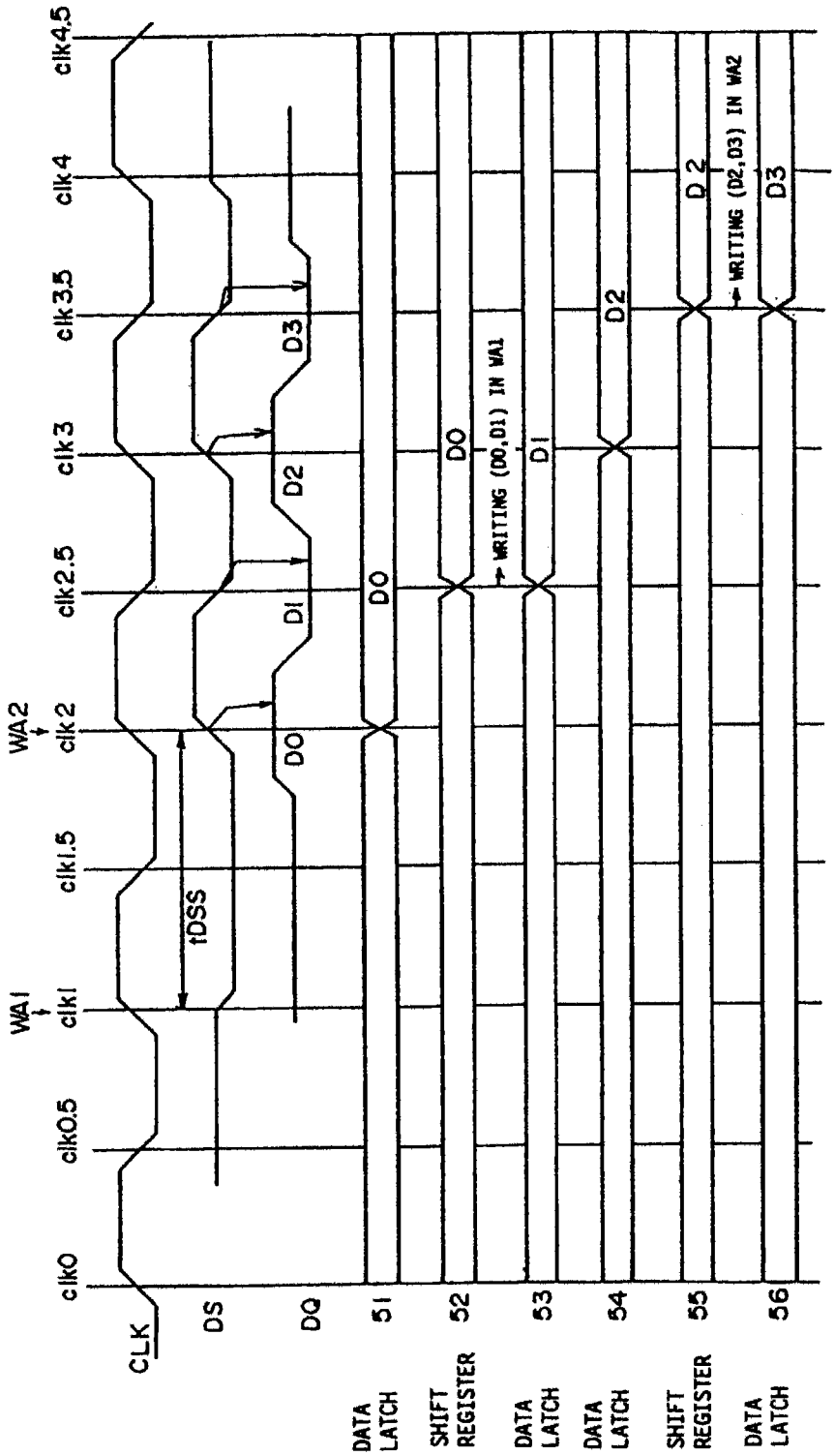

clk4.5
clk4
clk3.5
clk3
clk2.5
WA2
clk2
clk1.5
WA1
clk1
clk0.5
clk0
CLK
DS
DQ
51
52
53
54
55
56
DATA LATCH
SHIFT REGISTER
DATA LATCH
DATA LATCH
SHIFT REGISTER
DATA LATCH
tDSS
D3
D2
D1
D0
WRITING (D0,D1) IN WA1
WRITING (D2,D3) IN WA2

FIG.15

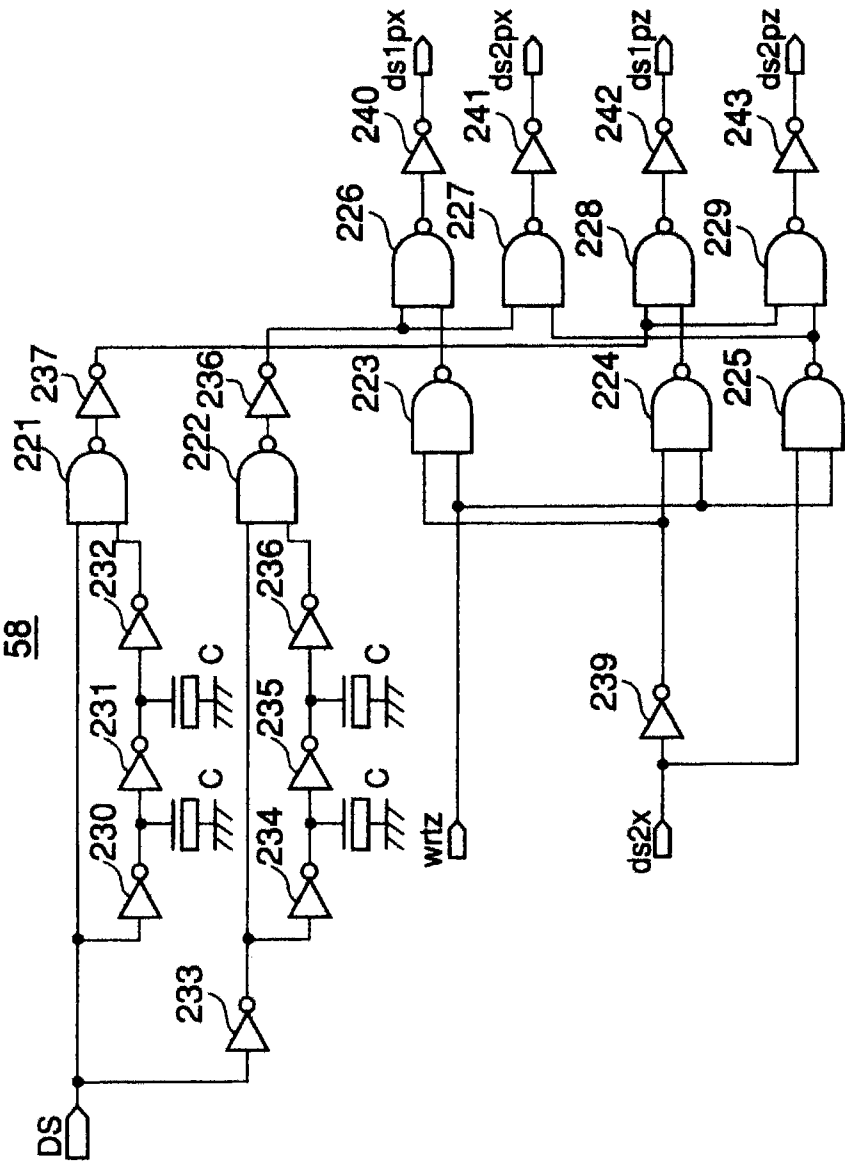

ds1px
ds2px
ds1pz
ds2pz
240
241
242
243
226
227
228
229
237
236
223
224
225
221
222
58
232
236
231
235
230
234
C
239
wrtz
ds2x
233
DS

FIG.16

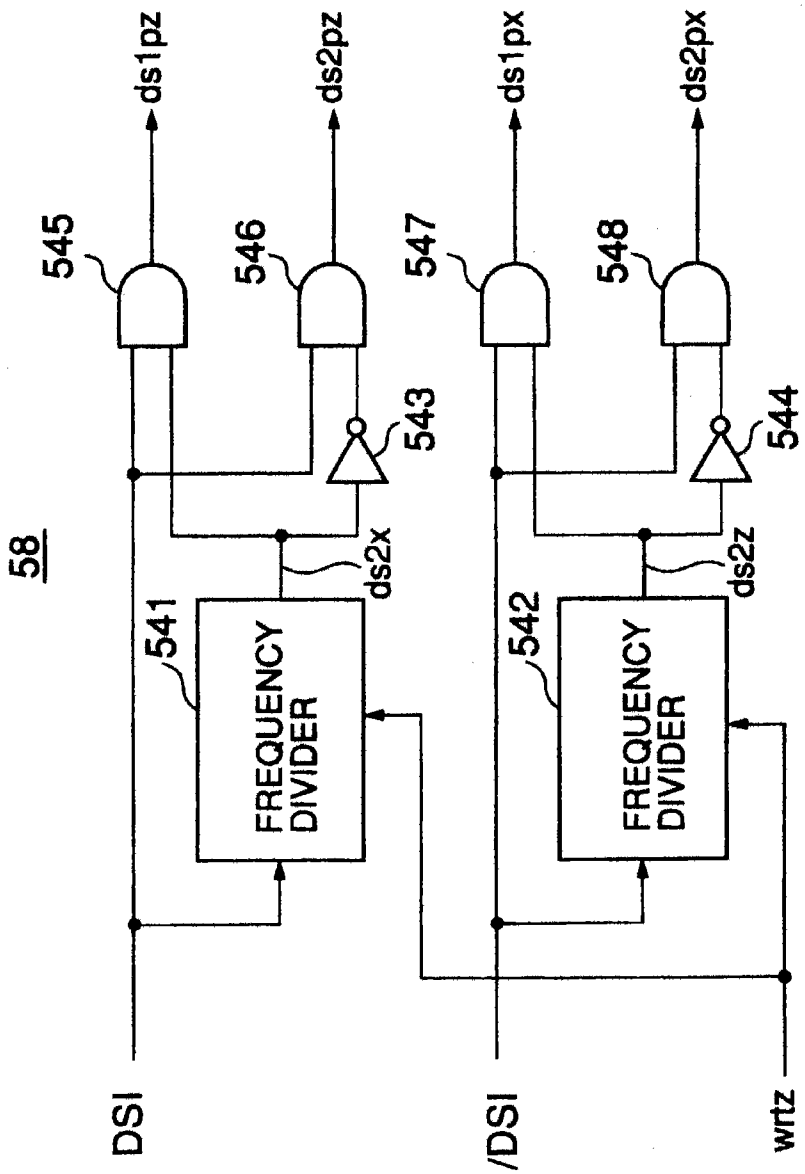

58
ds1pz
ds2pz
ds1px
ds2px
545
546
547
548
543
544
ds2x
ds2z
541
542
FREQUENCY DIVIDER
FREQUENCY DIVIDER
DSI
/DSI
wrtz

FIG.17

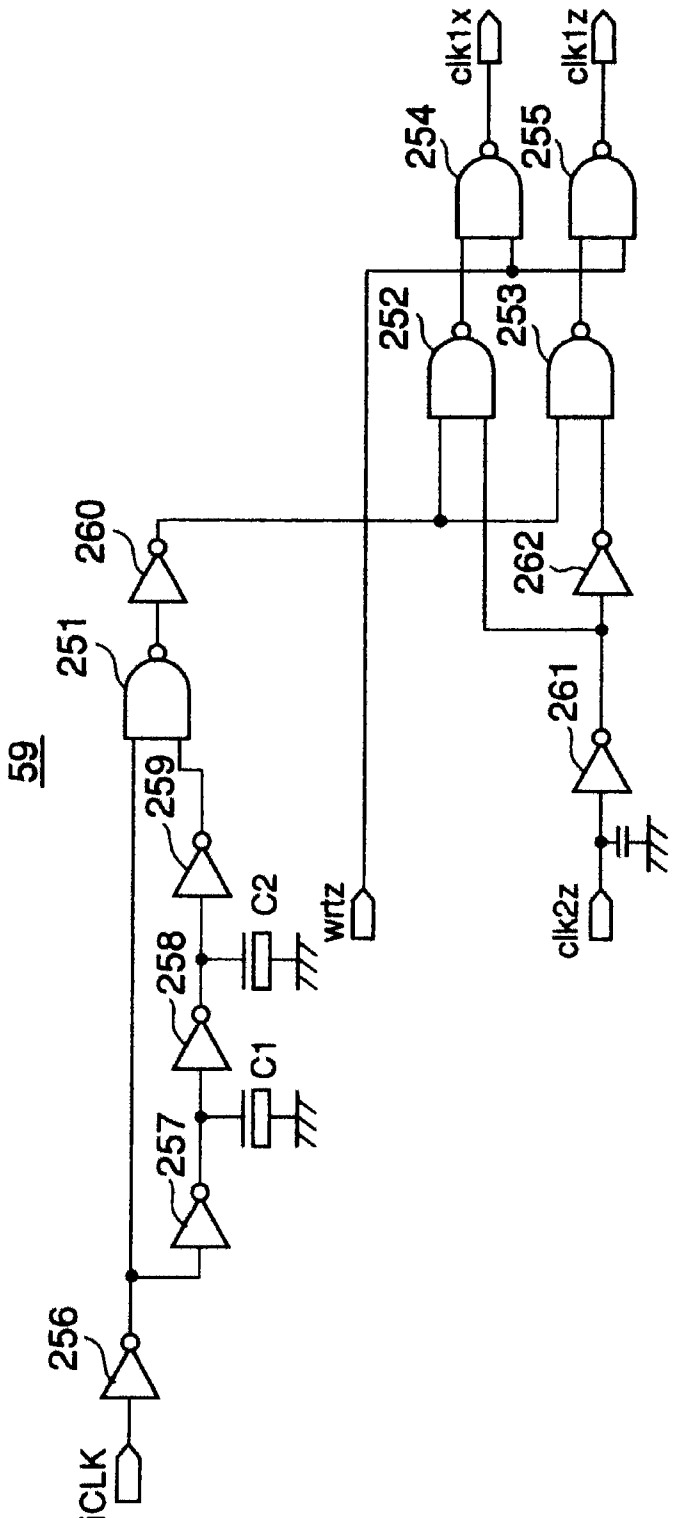

clk1x
clk1z
254
255
252
253
260
262
251
59
261
259
C2
wrtz
clk2z
258
C1
257
256
iCLK

FIG.18

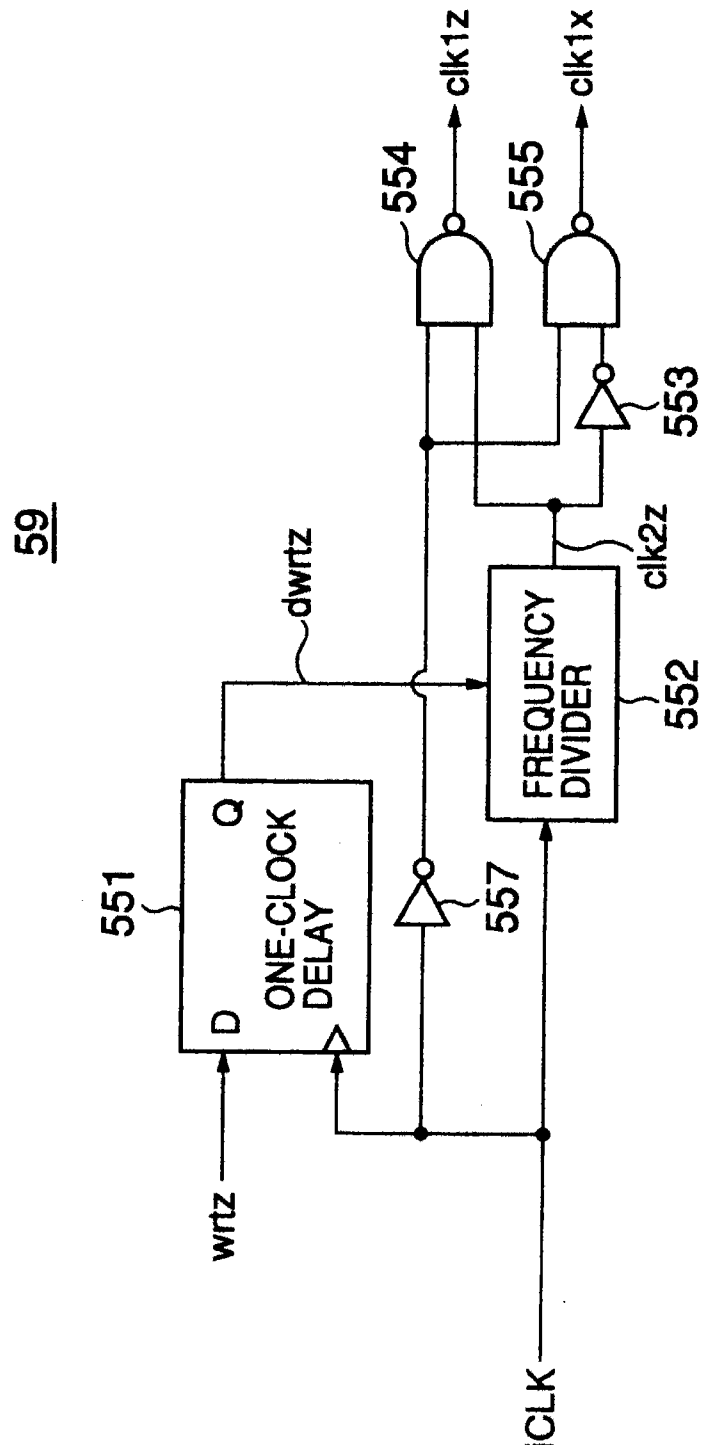

59
clk1z
clk1x
554
555
553
clk2z
dwrtz
FREQUENCY DIVIDER
552
551
Q
D
ONE-CLOCK DELAY
557
wrtz
iCLK

FIG.19

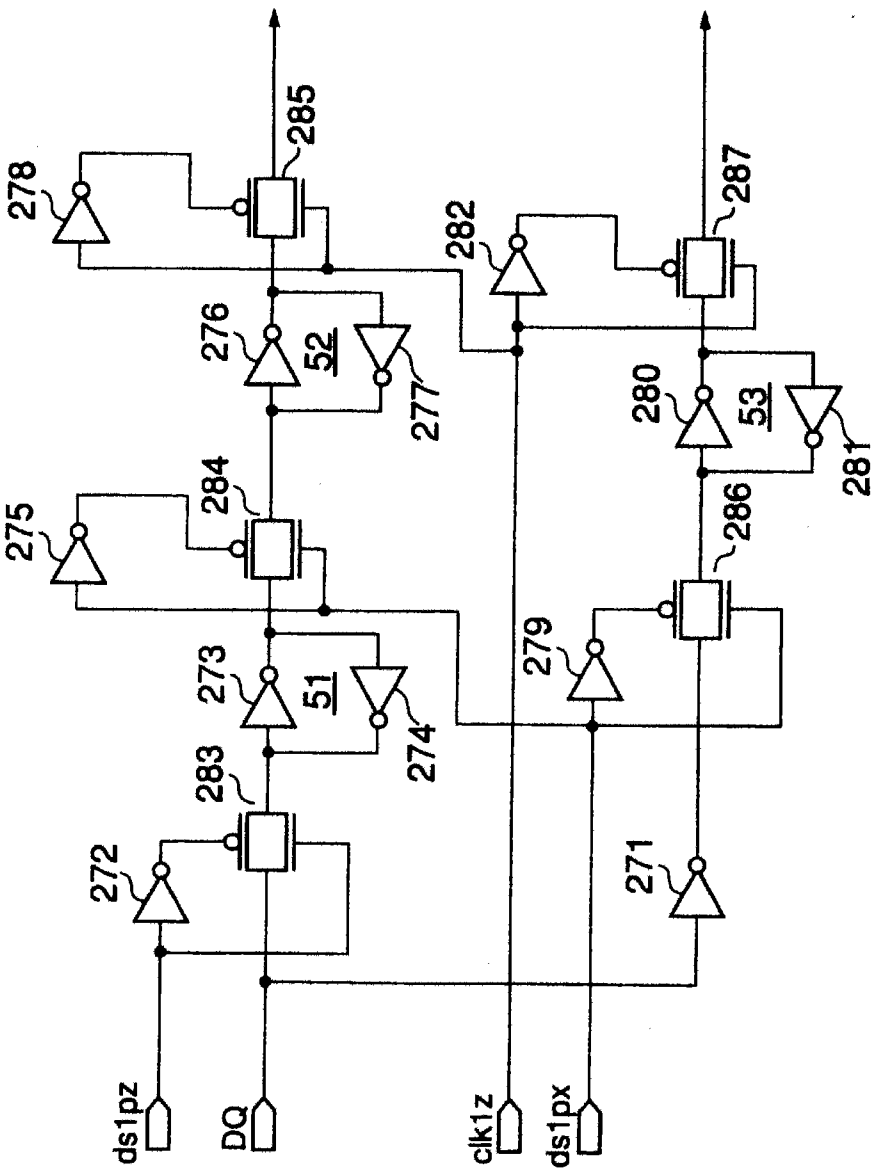

285
278
287
282
276
52
277
280
53
281
284
275
286
279
273
51
274
283
272
271
ds1pz
DQ
clk1z
ds1px

FIG.20

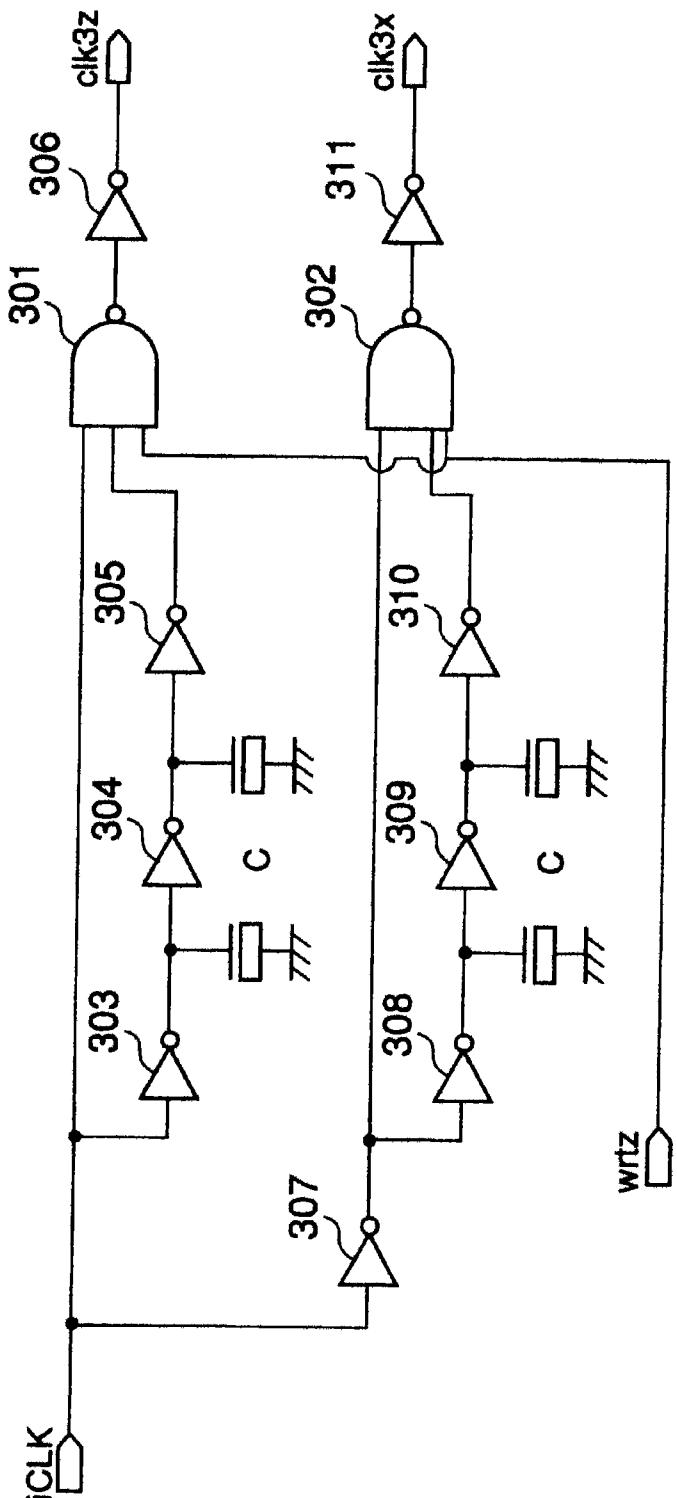

clk3z
clk3x
306
311
301
302
305
310
304
309
C
C
303
308
307
wrtz
iCLK

FIG.21

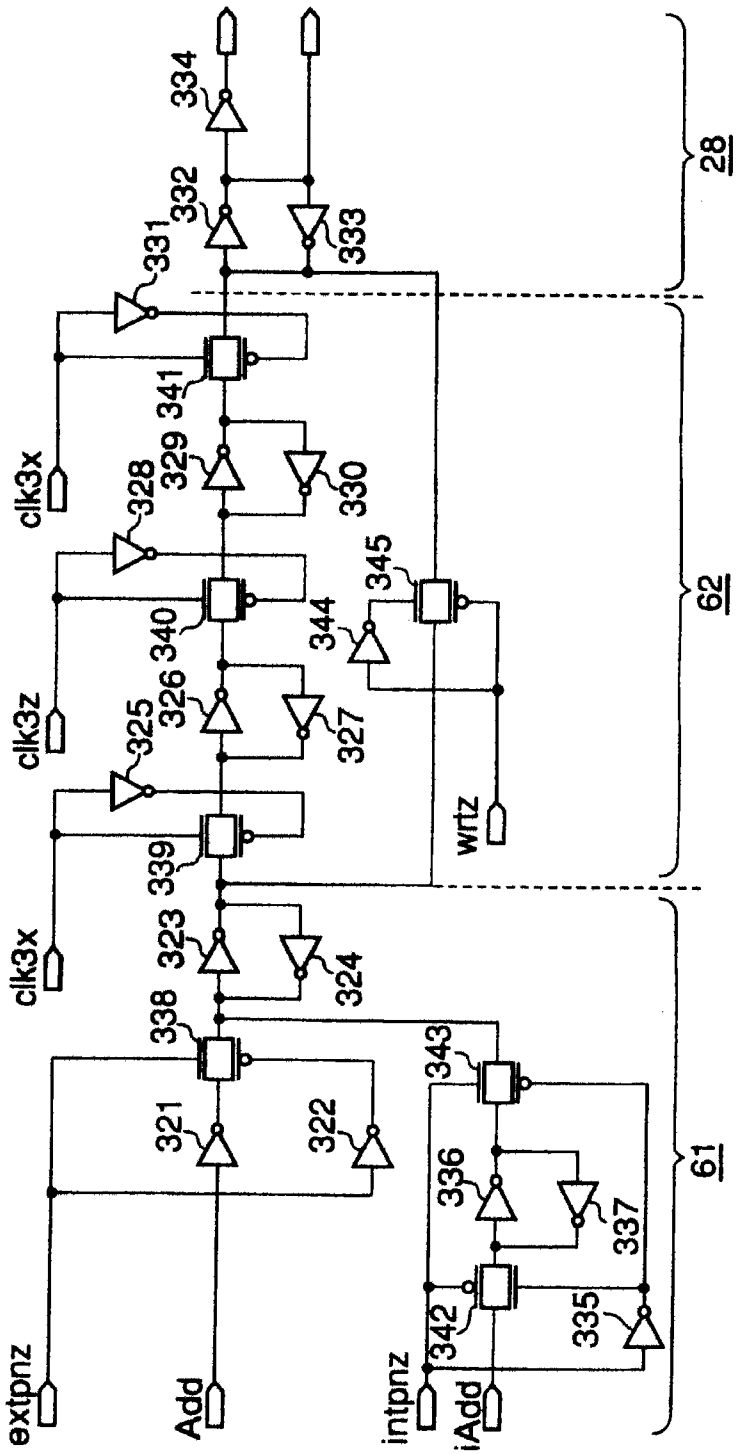

334
332
331
333
28
341
clk3x
328
329
330
345
340
344
62
clk3z
325
326
327
wrtz
339
clk3x
323
324
338
343
321
322
336
337
61
342
335
extpnz
Add
intpnz
iAdd

FIG.22

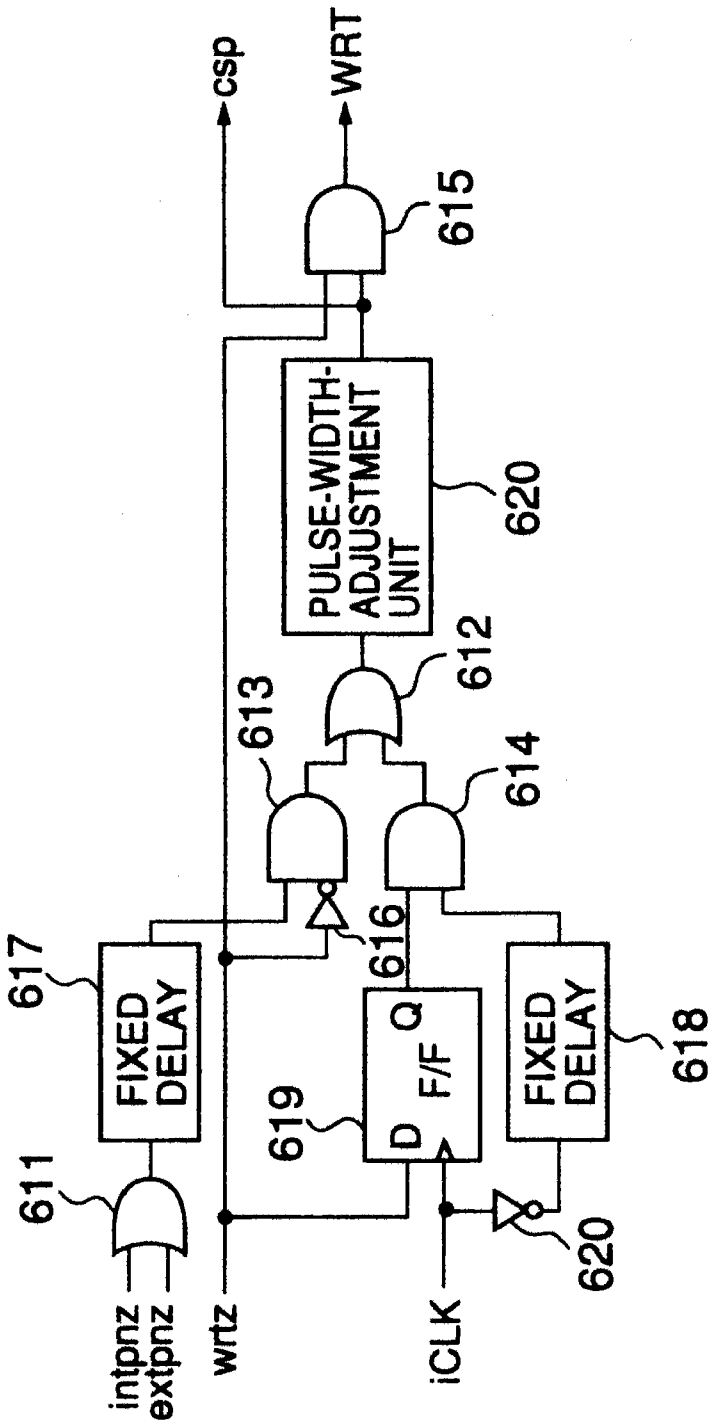
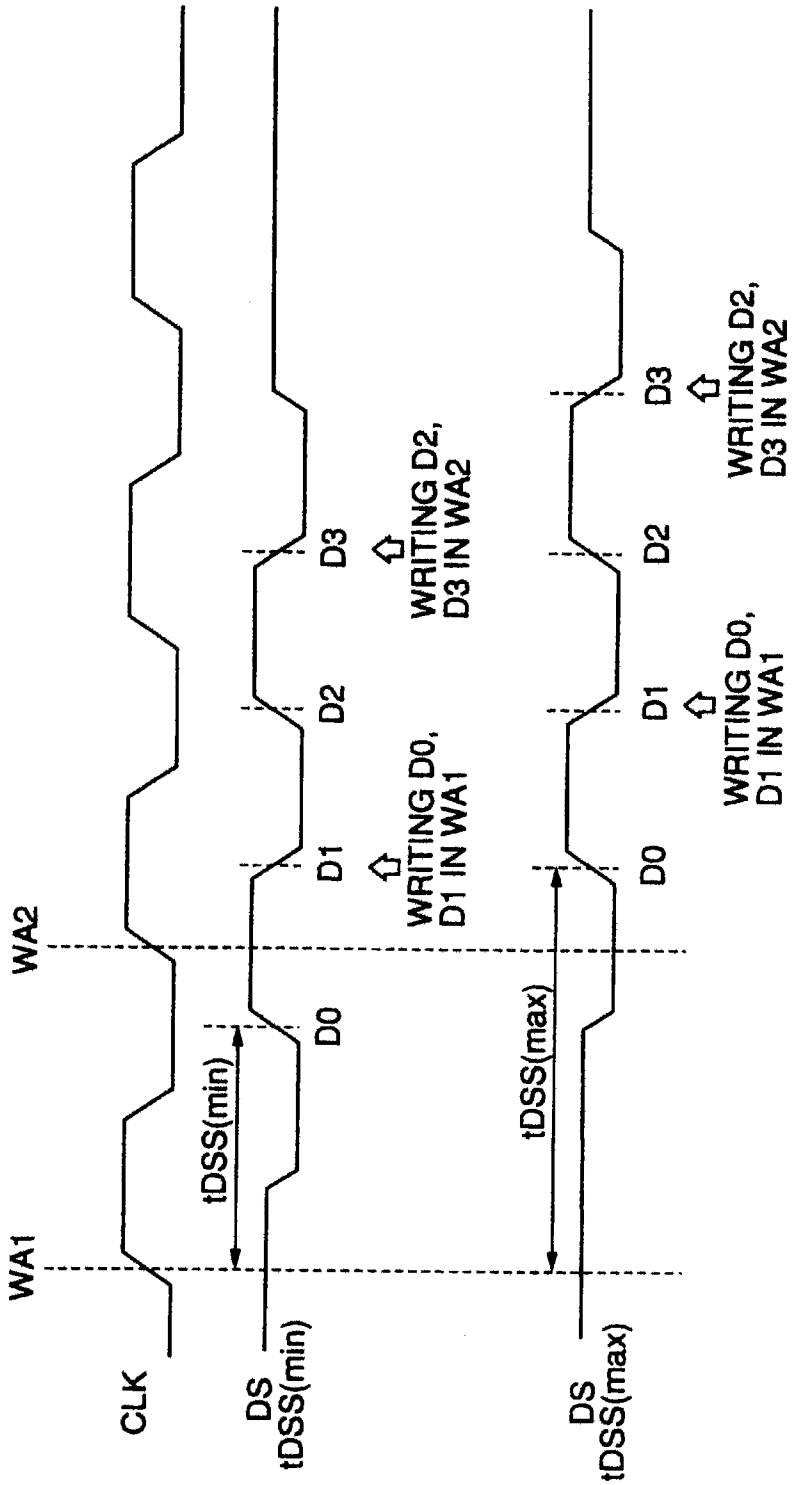

csp
WRT
615
PULSE-WIDTH-ADJUSTMENT UNIT
620
612
613
614
616
617
FIXED DELAY
D
Q
F/F
619
FIXED DELAY
618
611
620
intpnz
extpnz
wrtz
iCLK

FIG.23


CLK
WA1
WA2
DS
tDSS(min)
tDSS(min)
D0
D1
D2
D3
WRITING D0,
D1 IN WA1
WRITING D2,
D3 IN WA2
DS
tDSS(max)
tDSS(max)
D0
D1
D2
D3
WRITING D0,
D1 IN WA1
WRITING D2,
D3 IN WA2

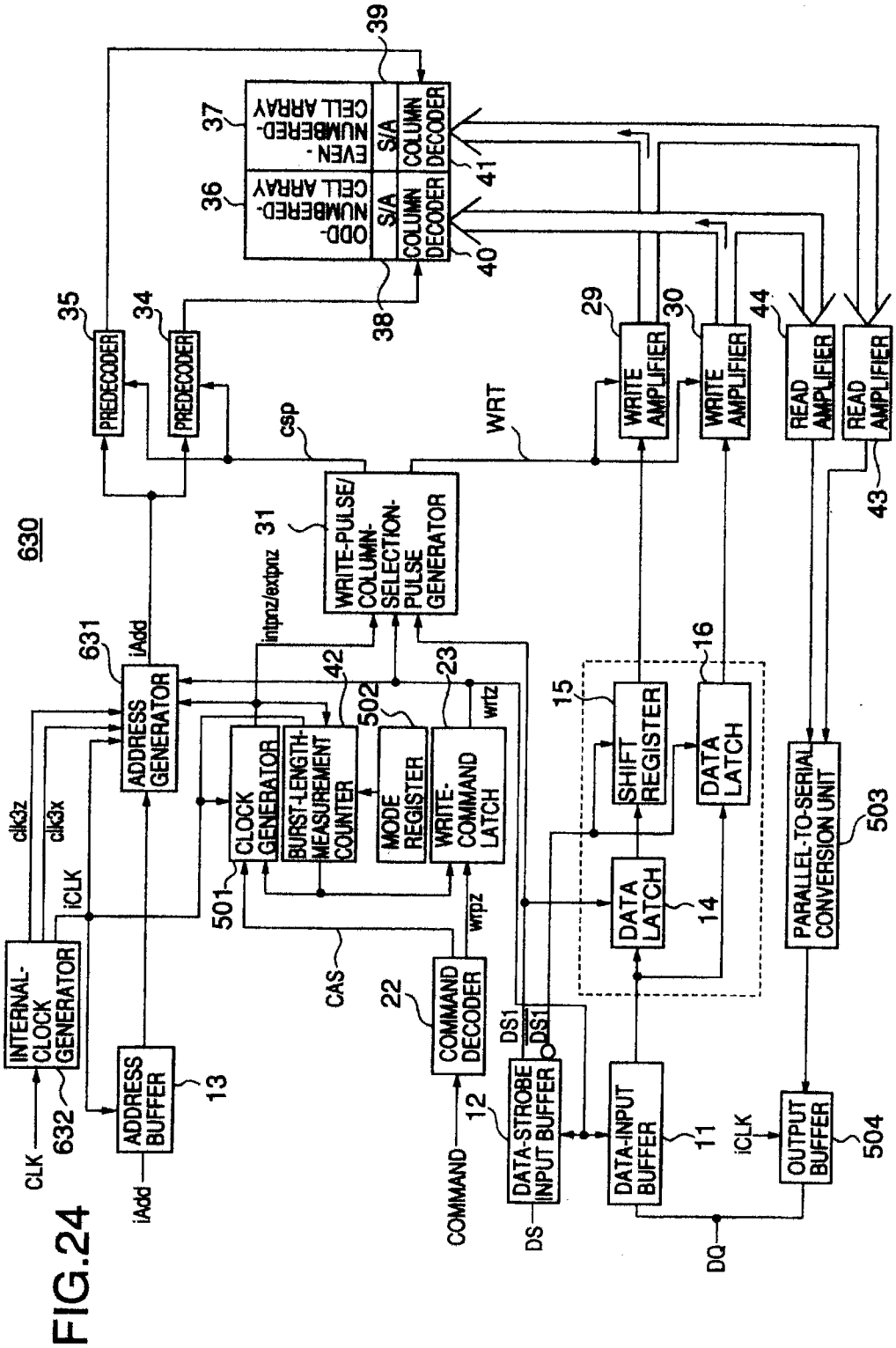

630
631
ADDRESS GENERATOR
iAdd
INTERNAL-CLOCK GENERATOR
clk3z
clk3x
iCLK
CLK
632
ADDRESS BUFFER
13
CLOCK GENERATOR
BURST-LENGTH-MEASUREMENT COUNTER
501
MODE REGISTER
502
WRITE-COMMAND LATCH
wrtz
wrtpz
CAS
22
COMMAND DECODER
COMMAND
12
DATA-STROBE INPUT BUFFER
DS
DS1
DS1
DATA-INPUT BUFFER
11
DQ
iCLK
OUTPUT BUFFER
504
PARALLEL-TO-SERIAL CONVERSION UNIT
503
SHIFT REGISTER
15
DATA LATCH
16
DATA LATCH
14
WRITE AMPLIFIER
29
WRITE AMPLIFIER
30
READ AMPLIFIER
44
READ AMPLIFIER
43
WRT
csp
WRITE-PULSE/ COLUMN-SELECTION-PULSE GENERATOR
31
intpnz/extpnz
42
23
PREDECODER
35
PREDECODER
34
38
39
ODD-NUMBERED-CELL ARRAY
36
S/A
COLUMN DECODER
40
EVEN-NUMBERED-CELL ARRAY
37
S/A
COLUMN DECODER
41

FIG.24

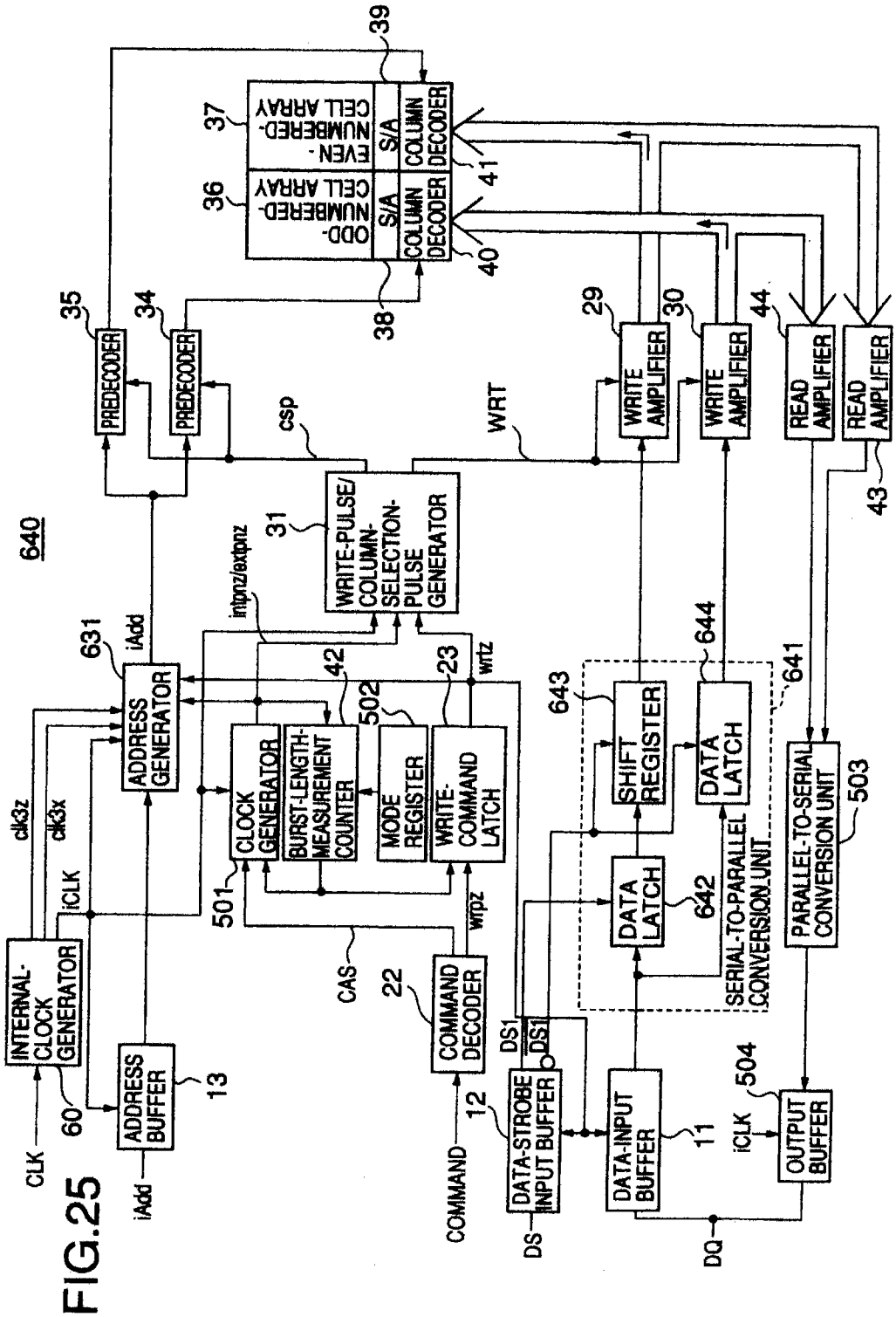

640
39
37
EVEN-NUMBERED-CELL ARRAY
S/A
COLUMN DECODER
41
36
ODD-NUMBERED-CELL ARRAY
S/A
COLUMN DECODER
40
38
35
PREDECODER
34
PREDECODER
csp
WRT
29
WRITE AMPLIFIER
30
WRITE AMPLIFIER
44
READ AMPLIFIER
READ AMPLIFIER
43
31
WRITE-PULSE/COLUMN-SELECTION-PULSE GENERATOR
intpnz/extpnz
631
iAdd
ADDRESS GENERATOR
42
23
wrtz
502
CLOCK GENERATOR
BURST-LENGTH-MEASUREMENT COUNTER
MODE REGISTER
WRITE-COMMAND LATCH
501
wrpz
CAS
22
COMMAND DECODER
643
SHIFT REGISTER
644
DATA LATCH
641
642
DATA LATCH
SERIAL-TO-PARALLEL CONVERSION UNIT
PARALLEL-TO-SERIAL CONVERSION UNIT
503
clk3z
clk3x
iCLK
INTERNAL-CLOCK GENERATOR
60
CLK
ADDRESS BUFFER
13
iAdd
DS1
DS1
12
COMMAND
DATA-STROBE INPUT BUFFER
DS
DATA-INPUT BUFFER
11
DQ
504
iCLK
OUTPUT BUFFER

FIG.25